

ABSTRACT

High frequency continuous-time circuits and built-in-self-test using CMOS RMS detector

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The expanding wireless market has resulted in complex integrated transceivers that involve RF, analog and mixed-signal circuits, resulting in expensive and complicated testing. The most important challenges that test engineering faces today are (1) providing a fast and accurate fault-diagnosis and performance characterization so as to accelerate the time-to-market and (2) providing an inexpensive test strategy that can be integrated with the design so as to aid the high-volume manufacturing process. The first part of the research focuses on the design of an RMS detector for built-in-self-test (BIST) of an RF integrated transceiver that can directly provide information at various test points in the design. A cascode low noise amplifier (LNA) has been chosen as the device under test (DUT). A compact ($< 0.031 \text{ mm}^2$) RF RMS detector with negligible input capacitance ($< 13 \text{ fF}$) has been implemented in $0.35 \text{ } \mu\text{m}$ CMOS technology along with the DUT. Experimental results are currently being assimilated and compared with the simulation results. Frequency limitations were encountered during the testing process due to unexpected increase in the value of the N-well resistors. All other problems faced during the testing, as well as the results obtained so far, are presented in this thesis. In the second part of the research, the use of the RMS detector for BIST has been extended to a continuous-time high-frequency boost-filter. The proposed HF RMS detector has been implemented along with a 24 dB 350 MHz boost filter as the DUT on $0.35 \text{ } \mu\text{m}$ CMOS technology. The HF RMS detector occupies 0.07 mm^2 and has an input capacitance of 7 fF . The HF RMS detector has a dynamic range greater than 24 dB starting from -38 dBm of input power. The bandwidth and boost of the filter have been accurately estimated in simulation using the HF RMS detector. The sensitivity of an intermediate band pass node of the filter has also been monitored to predict the filter's sensitivity to Q errors. The final part of the research describes the design of a single-ended to differential converter for use in a broadband transceiver operating from 50-850 MHz. This circuit is used as the second stage in the transceiver after the LNA. The design has been simulated on a $0.35 \text{ } \mu\text{m}$ CMOS process and has a power consumption of 13.5 mW and less than 8 dB of noise figure over the entire band. It is capable of driving a 500 fF load with less than 1dB of gain ripple over the entire band (50-850 MHz).