# ABSTRACT

Design of a 3.1-4.8 GHz RF Front-end for an Ultra Wideband Receiver (May 2005)
Pushkar Sharma, B.E. (Hons.) Panjab University, India
Chair of Advisory Committee: Dr. Aydin I. Karsilayan

IEEE 802.15 High Rate Alternative PHY task group (TG3a) is working to define a protocol for Wireless Personal Area Networks (WPANs) which makes it possible to attain data rates of greater than 110Mbps. Ultra Wideband (UWB) technology utilizing frequency band of 3.168 GHz – 10.6 GHz is an emerging solution to this with data rates of 110, 200 and 480 Mbps. Initially, UWB mode I devices using only 3.168 GHz – 4.752 GHz have been proposed. This frequency band is divided into three sub-bands of 528 MHz each.

Low Noise Amplifier (LNA) and I-Q Mixers are key components constituting the RF front-end. Performance of these blocks is very critical to the overall performance of the receiver. In general, main considerations for the LNA are low noise, 50Ω broadband input matching, high gain with maximum flatness and good linearity. For the mixers, it is essential to attain low flicker noise performance coupled with good conversion gain.
Proposed LNA architecture is a derivative of inductive source degenerated topology. Broadband matching at the LNA output is achieved using LC band-pass filter. To obtain high gain with maximum flatness, an LC band-pass filter is used at its output. Proposed LNA achieved a gain of 15dB, noise figure of less than 2.6dB and IIP3 of more than -7dBm.

Mixer is a modified version of double balanced Gilbert-cell topology where both I and Q channel mixers are merged together. Frequency response of each sub-band is matched by using an additional inductor, which further improves the noise figure and convergence gain. Current bleeding scheme is used to further reduce the low frequency noise. Mixer achieves average conversion gain of 14.5dB, IIP3 more than 6dBm and Double Side Band (DSB) noise figure less than 9dB. Maximum variation in conversion gain is desired to be less than 1dB. Both LNA and mixers are designed to be fabricated in TSMC 0.18μm CMOS technology.