ABSTRACT

A CMOS 500 MHz Continuous-Time Fourth Order 0.05° Equiripple
Linear Phase Filter with Automatic Tuning. (May 2003)
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The growing demand of portable electronic equipment and system-on-a-chip has been pushing the industry to design circuits with very low power supply voltage and low power consumption. The Hard Disk drive industry is looking for developments in the read channel chip to push the data rates to higher speed, along with a low voltage and low cost solution. Read channel requires high-speed linear phase filters to meet these objectives. The primary objective of this project is to design, layout, and characterize a4th-order continuous-time equiripple linear phase filter with automatic tuning system. The main requirements for design are high speed, low group delay variations, good linearity and power efficiency.

This filter features wide cut-off frequency 500MHz, which is far beyond the current state-of-the-art. The linear phase filter is based on Gm-C biquadratics. Higher speed has been achieved by minimizing the parasitics and a complementary input stage OTA. A common mode feedback (CMFB), which ensures stability at such high frequencies, has also been designed. The inaccuracies of the filter are compensated by using a simple automatic tuning system.

The design is fabricated in 0.35 μ TSMC CMOS process technology. The design was simulated in Cadence using SPICE models provided by MOSIS for the 0.35 μ TSMC process in the presence of parasitic capacitance and transistor non- idealities. Cut-off frequency of 500 MHz was achieved along with a 9% variation in the group delay.