ABSTRACT

A 1Gsample/s 6-bit flash A/D converter with a combined chopping and averaging technique for reduced distortion in 0.18µm CMOS

(May 2005)

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Hard disk drive applications require a high Spurious Free Dynamic Range (SFDR), 6-bit Analog-to-Digital Converter (ADC) at conversion rates of 1GHz and beyond. This work proposes a robust, fault-tolerant scheme to achieve high SFDR in an averaging flash A/D converter using comparator chopping. Chopping of comparators in a flash A/D converter was never previously implemented due to lack of feasibility in implementing multiple, uncorrelated, high speed random number generators. This work proposes a novel array of uncorrelated truly binary random number generators working at 1GHz to chop all comparators. Chopping randomizes the residual offset left after averaging, further pushing the dynamic range of the converter. This enables higher accuracy and lower bit-error rate for high speed disk-drive read channels. Power consumption and area are reduced because of the relaxed design requirements for the same linearity. The technique has been verified in Matlab simulations for a 6-bit 1Gsamples/s flash ADC under case of process gradients with non-zero mean offsets as high as 60mV and potentially serious spot offset errors as high as 1V for a 2V peak to peak input signal. The proposed technique exhibits an improvement of over 15dB compared to pure averaging flash converters for all cases. The circuit-level simulation results, for a 1V peak to peak input signal, demonstrate superior performance. The reported ADC was fabricated in TSMC 0.18µm CMOS process. It occupies 8.79mm2 and consumes about 400mW from 1.8V power supply at 1GHz. The targeted SFDR performance for the fabricated chip is at least 45dB for a 256MHz input sine wave, sampled at 1GHz, about 10dB improvement on the 6-bit flash ADCs in the literature.