ABSTRACT

Design methodologies for built-in testing of integrated RF transceivers with the on-chip loopback technique

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Marvin Olufemi Onabajo

Chair of Advisory Committee: Jose Silva-Martinez

Advances toward increased integration and complexity of radio frequency (RF) andmixed-signal integrated circuits reduce the effectiveness of contemporary testmethodologies and result in a rising cost of testing. The focus in this research is on thecircuit-level implementation of alternative test strategies for integrated wirelesstransceivers with the aim to lower test cost by eliminating the need for expensive RFequipment during production testing.The first circuit proposed in this thesis closes the signal path between the transmitterand receiver sections of integrated transceivers in test mode for bit error rate analysis atlow frequencies. Furthermore, the output power of this on-chip loopback block wasmade variable with the goal to allow gain and 1-dB compression point determination forthe RF front-end circuits with on-chip power detectors. The loopback block is intendedfor transceivers operating in the 1.9-2.4GHz range and it can compensate for transmitterreceiveroffset frequency differences from 40MHz to 200MHz. The measuredattenuation range of the 0.052mm2 loopback circuit in 0.13µm CMOS technology was 26-41dB with continuous control, but post-layout simulation results indicate that theattenuation range can be reduced to 11-27dB via optimizations.Another circuit presented in this thesis is a current generator for built-in testing ofimpedance-matched RF front-end circuits with current injection. Since this circuit hashigh output impedance (>1k up to 2.4GHz), it does not influence the input matchingnetwork of the low-noise amplifier (LNA) under test. A major advantage of the currentinjection method over the typical voltage-mode approach is that the built-in test canexpose fabrication defects in components of the matching network in addition to on-chipdevices. The current generator was employed together with two power detectors in arealization of a built-in test for a LNA with 14% layout area overhead in 0.13µm CMOStechnology (<1.5% for the 0.002mm2 current generator). The post-layout simulationresults showed that the LNA gain (S21) estimation with the external matching networkwas within 3.5% of the actual gain in the presence of process-voltage-temperaturevariations and power detector imprecision.