ABSTRACT

Low power architecture and circuit techniques for high boost wideband Gm-C filters

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With the current trend towards integration and higher data rates, read channel design needs to incorporate significant boost for a wider signal bandwidth. This dissertation explores the analog design problems associated with design of such 'Equalizing Filter' (boost filter) for read channel applications. Specifically, a 330MHz, 5th order Gm-C continuous time lowpass filter with 24dB boost is designed. Existing architectures are found to be unsuitable for low power, wideband and high boost operation. The proposed solution realizes boosting zeros by efficiently combining available transfer functions associated with all nodes of cascaded biquad cells. Further, circuit techniques suitable for high frequency filter design are elaborated such as: application of the Gilbert cell as a variable transconductor and a new Common-Mode-Feedback (CMFB) error amplifier that improves common mode accuracy without compromising on bandwidth or circuit complexity. A prototype is fabricated in a standard 0.35mm CMOS process. Experimental results show -41dB of IM3 for 250mV peak to peak swing with 8.6mW/pole of power dissipation.