

Abstract

Implementation of a 1GHZ frontend using transform domain charge sampling techniques sampling receivers

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Mandar Kulkarni

Chair of Advisory Committee: Sebastian Hoyos

The recent popularity and convenience of Wireless communication and the need for integration demands the development of Software Defined Radio (SDR). First defined by Mitola, the SDR processed the entire bandwidth using a high resolution and high speed ADC and remaining operations were done in DSP. The current trend in SDRs is to design highly reconfigurable analog front ends which can handle narrow-band and wideband standards, one at a time. Charge sampling has been widely used in these architectures due to the built in antialiasing capabilities, jitter robustness at high signal frequencies and flexibility in filter design. This work proposed a 1GHz wideband front end aimed at SDR applications using Transform Domain (TD) sampling techniques. Frequency Domain (FD) sampling, a special case of TD sampling, efficiently parallelizes the signal for digital processing, relaxing the sampling requirements and enabling parallel digital processing at a much lower rate and is a potential candidate for SDR. The proposed front end converts the RF signal into current and then it is downconverted using passive mixers. The front end has five parallel paths, each acting on a part of the spectrum effectively parallelizing the front end and relaxing the requirements. An overlap introduced between successive integration windows for jitter robustness was exploited to create a novel sinc² downsample by two filter topology. This topology was compared to a conventional topology and found to be equivalent and area efficient by about 44%. The proposed topology was used as a baseband filter for all paths in the front end. The chip was sent for fabrication in 45nm technology. The active area of the chip was 6:6mm². The testing and measurement of the chip still remains to be done.