

A PROTOTYPE OF A NEW CLASS OF OVERSAMPLING ADC.

ABSTRACT

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Analog-to-digital (A/D) and digital-to-analog (D/A) converters are important blocks in signal processing system because they provide the link between the analog world and digital systems. Compared with Nyquist-rate data converters, oversampling data converters are more desirable for modern submicron technologies with low voltage supplies. Today, all existing oversampling modulators in popular use are derived from sigma-delta modulation. Stability is the most significant problem in the sigma-delta modulator, because the ultimate accuracy is limited by stability. As the aggressiveness of the design increases, the margin of stability diminishes rapidly.

This thesis presents the design and experimental results of the first prototype circuit implementation of the novel oversampling modulation scheme proposed by Dr. Takis Zourntos. This new class of oversampling modulators are theoretically stable. With less stability limitation, the new class of modulators can potentially achieve higher signal-to-noise ratio (SNR) or less power by designing the modulator more aggressively. This thesis describes the methods and procedures of how the new oversampling modulation theory is implemented into a circuit. Some novel circuit architectures are proposed in this modulator, such as a filter which can provide status outputs for the controller and realize arbitrary zeros and poles, comparators with synchronization latches to eliminate the effect of metastability, and a digital-to-analog converter (DAC) with current calibration circuits for high linearity.

A third-order continuous-time oversampling modulator employing 4-bit quantization is implemented in a 0.35- μm double-poly complementary metal oxide semiconductor (CMOS) technology, with a chip area of 2150 μm^2 . Simulation results show it achieves 83.7-dB peak SQNR, 90-dB dynamic range over a 500kHz input signal bandwidth, and 60 mW power consumption.