ABSTRACT

A 10Gb/s Full On-chip Bang-Bang Clock and Data Recovery System Using an Adaptive Loop Bandwidth Strategy

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In this work, a highly linear broadband Low Noise Amplifier (LNA) is presented. The linearity issue in broadband Radio Frequency (RF) front-end is introduced, followed by an analysis of the specifications and requirements of a broadband LNA through consideration of broadband, multi-standard front-end design. Metal-Oxide- Semiconductor Field-Effect Transistor (MOSFET) non-linearity characteristics cause linearity problems in the RF front-end system. To solve this problem, feedback and the Derivative Superposition Method linearized MOSFET. In this work, novel linearization approaches such as the constant current biasing and the Derivative Superposition Method using a triode region transistor improve linearization stability against Process, Supply Voltage, and Temperature (PVT) variations and increase high power input capability. After analyzing and designing a resistive feedback LNA, novel linearization methods were applied. A highly linear broadband LNA is designed and simulated in 65nm CMOS technology. Simulation results including PVT variation and the Monte Carlo simulation are presented. We obtained -10dB S11, 9.77dB S21, and 4.63dB Noise Figure with IIP3 of 19.18dBm for the designed LNA. As demand for higher bandwidth I/O grows, the front end design of serial link becomes significant to overcome stringent timing requirements on noisy and bandwidthlimited channels. As a clock reconstructing module in a receiver, the recovered clock quality of Clock and Data Recovery is the main issue of the receiver performance. However, from unknown incoming jitter, it is difficult to optimize loop dynamics to minimize steady-state and dynamic jitter. In this thesis a 10 Gb/s adaptive loop bandwidth clock and data recovery circuit with on-chip loop filter is presented. The proposed system optimizes the loop bandwidth adaptively to minimize jitter so that it leads to an improved jitter tolerance performance. This architecture tunes the loop bandwidth by a factor of eight based on the phase information of incoming data. The resulting architecture performs as good as a maximum fixed loop bandwidth CDR while tracking high speed input jitter and as good as a minimum fixed bandwidth CDR while suppressing wide bandwidth steady-state jitter. By employing a mixed mode predictor, high updating rate loop bandwidth adaptation is achieved with low power consumption. Another relevant feature is that it integrates a typically large off-chip filter using a capacitance multiplication technique that employs dual charge pumps. The functionality of the proposed architecture has been verified through schematic and behavioral model simulations. In the simulation, the performance of jitter tolerance is confirmed that the proposed solution provides improved results and robustness

to the variation of jitter profile. Its applicability to industrial standards is also verified by the jitter tolerance passing SONET OC-192 successfully.