ABSTRACT

Integrated Circuit Blocks for High Performance Baseband and RF Analog-to-Digital Converters

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Nowadays, the multi-standard wireless receivers and multi-format video processors have created a great demand for integrating multiple standards into a single chip. The multiple standards usually require several Analog to Digital Converters (ADCs) with different specifications. A promising solution is adopting a power and area efficient reconfigurable ADC with tunable bandwidth and dynamic range. The advantage of the reconfigurable ADC over customized ADCs is that its power consumption can be scaled at different specifications, enabling optimized power consumption over a wide range of sampling rates and resulting in a more power efficient design. Moreover, the reconfigurable ADC provides IP reuse, which reduces design efforts, development costs and time to market. On the other hand, software radio transceiver has been introduced to minimize RF blocks and support multiple standards in the same chip. The basic idea is to perform the analog to digital (A/D) and digital to analog (D/A) conversion as close to the antenna as possible. Then the backend digital signal processor (DSP) can be programmed to deal with the digital data. The continuous time (CT) bandpass (BP) sigma-delta ADC with good SNR and low power consumption is a good choice for the software radio transceiver. In this work, a proposed 10-bit reconfigurable ADC is presented and the non-overlapping clock generator and state machine are implemented in UMC 90nm CMOS technology. The state machine generates control signals for each MDAC stage so that the speed can be reconfigured, while the power consumption can be scaled. The measurement results show that the reconfigurable ADC achieved 0.6-200 MSPS speed with 1.9-27 mW power consumption. The ENOB is about 8 bit over the whole speed range. In the second part, a 2-bit quantizer with tunable delay circuit and 2-bit DACs are implemented in TSMC 0.13um CMOS technology for the 4th order CT BP sigma-delta ADC. The 2-bit quantizer and 2-bit DACs have 6dB SNR improvement and better stability over the single bit quantizer and DACs. The penalty is that the linearity of the feedback DACs should be considered carefully so that the nonlinearity doesn't deteriorate the ADC performance. The tunable delay circuit in the quantizer is designed to adjust the excess loop delay up to +/- 10% to achieve stability and optimal performance.