ABSTRACT

A Switched Capacitor, Fourth-Order Bandpass Sigma-Delta Modulator

for 20MHz IF Digitization. (May 2003)

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The past few years have witnessed an explosive growth of wireless applications for mobile communications and wireless networking. With modern sub-micron technologies, it is feasible to achieve complete integration of the RF transceiver chain in a low cost process such as CMOS. One possible way to accomplish this is to move the ADC closer to the incoming RF frequency. Bandpass $\Sigma\Delta$ modulators are ideally suited for digitizing narrow-band signals with bandwidth typically between 0-200KHz centered at higher intermediate frequencies from 20MHz to 200MHz. This mitigates errors such as mismatch, flicker noise and DC offset. Digitizing the weak signal at IF frequencies, requires high dynamic range and linearity from the ADC, due to the presence of strong interferers located close to in-band signals.

This report explains the design and layout of a fourth-order bandpass $\Sigma\Delta$ modulator implemented with switched-capacitor circuit in 0.35μm CMOS technology. The selected architecture for the $\Sigma\Delta$ modulator is the Cascade of Resonators (CRFB) topology with a 1-bit quantizer, having reference voltage of $\pm$ 250mV. The input applied has an amplitude of $\pm$125mV and frequency of 20MHz and the sampling frequency is 80MHz. Simulated results give a peak SNR at the output as 76dB for -6dB power of the input. The third-order non-linear products are suppressed by -55dB and power consumption of the modulator is 20mW.