ABSTRACT

High Performance Integrated Circuit Blocks for High-IF Wideband Receivers

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Due to the demand for high-performance radio frequency (RF) integrated circuit design in the past years, a system-on-chip (SoC) that enables integration of analog and digital parts on the same die has become the trend of the microelectronics industry. As a result, a major requirement of the next generation of wireless devices is to support multiple standards in the same chip-set. This would enable a single device to support multiple peripheral applications and services. Based on the aforementioned, the traditional superheterodyne front-end architecture is not suitable for such applications as it would require a complete receiver for each standard to be supported. A more attractive alternative is the highintermediate frequency (IF) radio architecture. In this case the signal is digitalized at an intermediate frequency such as 200MHz. As a consequence, the baseband operations, such as down-conversion and channel filtering, become more power and area efficient in the digital domain. Such architecture releases the specifications for most of the front-end building blocks, but the linearity and dynamic range of the ADC become the bottlenecks in this system. The requirements of large bandwidth, high frequency and enough resolution make such ADC very difficult to realize. Many ADC architectures were analyzed and Continuous-Time Bandpass Sigma-Delta (CT-BP-ΣΔ) architecture was found to be the most suitable solution in the high-IF receiver architecture since they combine oversampling and noise shaping to get fairly high resolution in a limited bandwidth. A major issue in continuous-time networks is the lack of accuracy due to powervoltage- temperature (PVT) tolerances that lead to over 20% pole variations compared to their discrete-time counterparts. An optimally tuned BP ΣΔ ADC requires correcting for center frequency deviations, excess loop delay, and DAC coefficients. Due to these undesirable effects, a calibration algorithm is necessary to compensate for these variations in order to achieve high SNR requirements as technology shrinks. In this work, a novel linearization technique for a Wideband Low-Noise Amplifier (LNA) targeted for a frequency range of 3-7GHz is presented. Post-layout simulations show NF of 6.3dB, peak S21 of 6.1dB, and peak IIP3 of 21.3dBm, respectively. The power consumption of the LNA is 5.8mA from 2V. Secondly, the design of a CMOS 6th order CT BP-ΣΔ modulator running at 800 MHz for High-IF conversion of 10MHz bandwidth signals at 200 MHz is presented. A novel transconductance amplifier has been developed to achieve high linearity and high dynamic range at high frequencies. A 2-bit quantizer with offset cancellation is alsopresented. The sixth-order modulator is implemented using 0.18 um TSMC standard analog CMOS technology. Post-layout simulations in cadence demonstrate that the modulator achieves a SNDR of 78 dB (~13 bit) performance

over a 14MHz bandwidth. The modulator's static power consumption is 107mW from a supply power of ± 0.9V. Finally, a calibration technique for the optimization of the Noise Transfer Function CT BP ΣΔ modulators is presented. The proposed technique employs two test tones applied at the input of the quantizer to evaluate the noise transfer function of the ADC, using the capabilities of the Digital Signal Processing (DSP) platform usually available in mixed-mode systems. Once the ADC output bit stream is captured, necessary information to generate the control signals to tune the ADC parameters for best Signal-to-Quantization Noise Ratio (SQNR) performance is extracted via Least- Mean Squared (LMS) software-based algorithm. Since the two tones are located outside the band of interest, the proposed global calibration approach can be used online with no significant effect on the in-band content.