ABSTRACT

Design of high speed low voltage data converters for UWB communication systems

(May 2006)

Choong Hoon Lee

Chair of Advisory Committee: Aydin Karsilayan

For A/D converters in ultra-wideband (UWB) communication systems, the flash A/D type is commonly used because of its fast speed and simple architecture. However, the number of comparators in a flash A/D converter exponentially increases with an increase in resolution; therefore, an interpolating technique is proposed in this thesis to mitigate the exponential increase of comparators in a flash converter. The proposed structure is designed to improve the system bandwidth degradation by replacing the buffers and resistors of a typical interpolating technique with a pair of transistors. This replacement mitigates the bandwidth degradation problem, which is the main drawback of a typical interpolating A/D converter. With the proposed 4-bit interpolating structure, 3.75 of effective number of bits (ENOB) and 31.52dB of spurious-free dynamic range (SFDR) are achieved at Nyquist frequency of 264MHz with 6.93mW of power consumption. In addition, a 4-bit D/A converter is also designed for the transmitter part of the UWB communication system. The proposed D/A converter is based on the charge division reference generator topology due to its full swing output range, which is attractive for low-voltage operation. To avoid the degradation of system bandwidth, resistors are replaced with capacitors in the charge division topology. With the proposed D/A converter, 0.26 LSB of DNL and 0.06 LSB of INL is obtained for the minimum input data stream width of 1.88ns. A 130 Âµm Ã—286 Âµm chip area is required for the proposed D/A converter with 19.04mW of power consumption. The proposed A/D and D/A converter are realized in a TSMC 0.18 Âµm CMOS process with a 1.8 supply voltage for the 528MHz system frequency.