

ABSTRACT

Design and Implementation of Low Power Multistage Amplifiers and High Frequency
Distributed Amplifiers.

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The advancement in integrated circuit (IC) technology has resulted in scaling down of device sizes and supply voltages without proportionally scaling down the threshold voltage of the MOS transistor. This, coupled with the increasing demand for low power, portable, battery-operated electronic devices, like mobile phones, and laptops provides the impetus for further research towards achieving higher integration on chip and low power consumption. High gain, wide bandwidth amplifiers driving large capacitive loads serve as error amplifiers in low-voltage low drop out regulators in portable devices. This demands low power, low area, and frequency-compensated multistage amplifiers capable of driving large capacitive loads. The first part of the research proposes two power and area efficient frequency compensation schemes: Single Miller Capacitor Compensation (SMC) and Single Miller Capacitor Feedforward Compensation (SMFFC), for multistage amplifiers driving large capacitive loads. The designs have been implemented in a $0.5\mu\text{m}$ CMOS process. Experimental results show that the SMC and SMFFC amplifiers achieve gain-bandwidth products of 4.6MHz and 9MHz, respectively, when driving a load of $25\text{K}\Omega/120\text{pF}$. Each amplifier operates from a

$\pm 1\text{V}$ supply, dissipates less than 0.42mW of power and occupies less than 0.02mm^2 of silicon area.

The inception of the latest IEEE standard like IEEE 802.16 wireless metropolitan area network (WMAN) for 10 - 66 GHz range demands wide band amplifiers operating at high frequencies to serve as front-end circuits (e.g. low noise amplifier) in such receiver architectures. Devices used in cascade (multistage amplifiers) can be used to increase the gain but it is achieved at an expense of bandwidth. Distributing the capacitance associated with the input and the output of the device over a ladder structure (which is periodic), rather than considering it to be lumped can achieve an extension of bandwidth without sacrificing gain. This concept which is also known as distributed amplification has been explored in the second part of the research. This work proposes certain guidelines for the design of distributed low noise amplifiers operating at very high frequencies. Noise analysis of the distributed amplifier with real transmission lines is introduced. The analysis for gain and noise figure is verified with simulation results from a 5-stage distributed amplifier implemented in a $0.18\mu\text{m}$ CMOS process.