ABSTRACT

Design Of A 20MHz Transimpedance Amplifier With Embedded Low-pass Filter For A Direct Conversion Wireless Receiver

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Charles Sekyiamah

Chair of Advisory Committee: Aydin Karsilayan

Accelerated growth in wireless communications in recent years has led to the emergence of portable devices that employ several wireless communication standards to provide multiple functionality such as cellular communication, wireless data communication and connectivity, entertainment and navigation, within the same device. Industry drive is towards reduction of the number of radio frequency (RF) front-end receivers required to cater to the various standards/bands within a single device to reduce cost, size and power consumption. The current trend is to use broadband/multi-standard or reconfigurable RF front-ends to cater to two or three standards at a time for cost-effective RF front-end solutions. The direct conversion receiver architecture has become attractive as it offers a full on-chip front-end solution without the need for expensive external components. Passive current-mode mixers are used in these receivers to eliminate mixer flicker noise. The inband current signals are typically in the micro-amp range after mixer downconversion. Transimpedance amplifiers are used to convert the downconverted current signals to voltage, and they provide amplification in the process. Because of the co-existence of multiple-radios within each device, large blocker currents downconvert close to the channel bandwidth after the mixer. Conventionally, single-pole transimpedance amplifier (TIA) filters are used to provide out-of-band (OOB) signal filtering. This requires high resolution analog-to-digital converters (ADCs) later in the receiver chain for signal processing. Providing higher order filtering before the ADC relaxes its specifications and this reduces the ADC and ADC calibration cost and complexity. Typically, an extra filtering stage is provided in the form of a cascaded filtering block after the single-pole TIA. In this work, higher order filtering is embedded within the TIA in the form of active feedback. In addition to relaxing the ADC specifications, this proposed TIA provides improved large signal linearity such as P1dB compression point. Furthermore, since the extra-circuitry is not in the signal path, in-band flicker noise and linearity are not degraded. The proposed TIA filter has been designed in IBM 90nm technology with a supply voltage of 1.2V. It can tolerate close-in blocker magnitudes of 4.5mA at 60MHz and higher before inband 1dB compression is reached.