ABSTRACT

Stability Issues in IC Low Drop Out

Voltage Regulators. (December 2002)

Krishna Chaitanya Chava, B.Tech., Indian Institute of Technology

Chair of Advisory Committee: Dr. Jose Silva-Martinez

Performance issues of IC Low Drop Out (LDO) voltage regulators, with specific reference to stability, are discussed in this thesis. Evaluation of existing frequency compensation schemes and their performances across operating loads is presented. The problem of instability of the LDO voltage regulator at low Electo Static Resistance (ESR) of the load capacitors and the consequences of this problem are highlighted. As a solution to some of the discussed problems, an alternate LDO voltage regulator topology that is stable with low Electro Static Resistance (ESR) capacitive loads is presented. The proposed scheme, instead of relying on the zero generated by the load capacitor and its ESR combination for stability, generates a zero internally. The LDO voltage regulator is implemented and fabricated in AMI 0.5μm CMOS technology through MOSIS service. It is demonstrated that this scheme realizes robust frequency compensation, facilitates use of Multi Layer Ceramic Capacitors (MLCC) for load of LDO regulators, and improves transient response and noise performance. Test results from the prototype provide an evaluation of the most important parameters of the regulator: ground current, load regulation, line regulation, output noise and start-up time.