# ABSTRACT

20 MHz IF Bandpass Switched Capacitor $\Sigma\Delta$ Modulator Using a
High Performance OTA with NCFF Compensation Scheme. (December 2001)
Bharath Kumar Thandri, B.E., Birla Institute of Technology and Science, Pilani, India
Chair of Advisory Committee: Dr. Jose Silva-Martinez

Switched capacitor (SC) circuits are widely used in many applications because of their accuracy and ease of integration in CMOS technology. They are not suitable for operation in high frequencies because of the settling time limitation of amplifiers. High frequency switched capacitor circuits pose challenging design specifications on the amplifiers which cannot be met by conventional circuit design techniques. High amplifier gain is required for an accurate output, whereas fast settling time is obtained by a high gainbandwidth (GBW) product. Amplifiers that use cascading of gain stages for obtaining high gain require some robust frequency compensation schemes, and usually have a low GBW, resulting in a slow settling time. This work proposes a new compensation scheme for high gain wideband amplifiers - No Capacitor Feed Forward (NCFF) compensation scheme. NCFF scheme uses pole-zero cancellation to obtain high gain, high GBW and a good phase margin. Left half plane (LHP) zeros produced due to the feedforward path causes a positive phase shift and is used to cancel the negative phase shift of poles. Fully differential and single ended operational transconductance amplifiers (OTA) using the proposed NCFF compensation scheme have been designed and fabricated using CMOS AMI 0.5$\mu$m technology. The fully differential OTA has a gain of 97 dB, GBW of 350 MHz and a phase margin of around $90^o$.

Sigma delta ($\Sigma\Delta$) modulators use oversampling and quantization noise shaping to obtain a high dynamic range. They are well suited for use in radio and cellular systems to directly convert the narrowband IF signal centered at high frequencies to digital domain. Switched capacitor implementation of a $\Sigma\Delta$ modulator requires a fast settling amplifier to operate at high IF frequencies. The design and implementation issues of a 20 MHz IF, 80 MHz clock, fourth order switched capacitor bandpass $\Sigma\Delta$ modulator are discussed in detail. The modulator uses a high performance OTA using the proposed NCFF compensation scheme and it has been designed and fabricated using 3.3V CMOS TSMC 0.35$\mu$m technology. The bandpass $\Sigma\Delta$ modulator has a peak SNR of 70 dB (post-layout simulations).