

# ABSTRACT

Self-calibrating random access logarithmic pixel for on chip camera

(May 2005)

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CMOS active pixel sensors (APS) have shown competitive performance with charge-coupled device (CCD) and offer many advantages in cost, system power reduction and on-chip integration of VLSI electronics. Among CMOS image sensors, sensors with logarithmic pixels are particularly applicable for outdoor environment where the light intensity varies over a wide range. They are also randomly accessible in both time and space. A major drawback comes from process variations during fabrication. This gives rise to a considerable fixed pattern noise (FPN) which deteriorates the image quality. In this thesis, a technique that greatly reduces FPN using on-chip calibration is introduced. An image sensor that consists of 64x64 active pixels has been designed, fabricated and tested. Pixel pitch is 18 $\mu\text{m}$  x 19.2 $\mu\text{m}$  and is fabricated in a 0.5- $\mu\text{m}$  CMOS process. The proposed pixel circuit considerably reduces the FPN as predicted in theoretical analysis. The measured FPN value is 2.29% of output voltage swing and column-wise FPN is 1.49% of mean output voltage over each column.