ABSTRACT

Nonlinearity and Noise Modeling of Operational Transconductance Amplifiers for Continuous Time Analog Filters. (May 2005)

Arun Ramachandran, B.En., Birla Institute of Technology and Science-Pilani, India;
M.S., Birla Institute of Technology and Science-Pilani, India
Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

A general framework for performance optimization of continuous-time OTA-C (Operational Transconductance Amplifier-Capacitor) filters is proposed. Efficient procedures for evaluating nonlinear distortion and noise valid for any filter of arbitrary order are developed based on the matrix description of a general OTA-C filter model . Since these procedures use OTA macromodels, they can be used to obtain the results significantly faster than transistor-level simulation. In the case of transient analysis, the speed-up may be as much as three orders of magnitude without almost no loss of accuracy. This makes it possible to carry out direct numerical optimization of OTA-C filters with respect to important characteristics such as noise performance, THD, IM3, DR or SNR. On the other hand, the general OTA-C filter model allows us to apply matrix transforms that manipulate (rescale) filter element values and/or change topology without changing its transfer function. The above features are a basis to build automated optimization procedures for OTA-C filters. In particular, a systematic optimization procedure using equivalence transformations is proposed. The research also proposes suitable software implementations of the optimization process. The first part of the research proposes a general performance optimization procedure and to verify the process two application type examples are mentioned. An application example of the proposed approach to optimal block sequencing and gain distribution of 8^{th} order cascade Butterworth filter (for two variants of OTA topologies) is given. Secondly the modeling tool is used to select the best suitable topology for a 5^{th} order Bessel Low Pass Filter. Theoretical results are verified by comparing to transistor-level simulation with

CADENCE. For the purpose of verification, the filters have also been fabricated in standard 0.5μm CMOS process.

The second part of the research proposes a new linearization technique to improve the linearity of an OTA using an Active Error Feedforward technique. Most present day applications require very high linear circuits combined with low noise and low power consumption. An OTA based biquad filter has also been fabricated in 0.35μm CMOS process. The measurement results for the filter and the stand alone OTA have been discussed. The research focuses on these issues.