

# ABSTRACT

Design techniques for low noise and high speed A/D converters

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Analog-to-digital (A/D) conversion is a process that bridges the real analog world to digital signal processing. It takes a continuous-time, continuous amplitude signal as its input and outputs a discrete-time, discrete-amplitude signal. The resolution and sampling rate of an A/D converter vary depending on the application. Recently, there has been a growing demand for broadband ( $>1$  MHz), high-resolution ( $>14$ bits) A/D converters. Applications that demand such converters include asymmetric digital subscriber line (ADSL) modems, cellular systems, high accuracy instrumentation, and medical imaging systems. This thesis suggests some design techniques for such high resolution and high sampling rate A/D converters. As the A/D converter performance keeps on increasing it becomes increasingly difficult for the input driver to settle to required accuracy within the sampling time. This is because of the use of larger sampling capacitor (increased resolution) and a decrease in sampling time (higher speed). So there is an increasing trend to have a driver integrated onchip along with A/D converter. The first contribution of this thesis is to present a new precharge scheme which enables integrating the input buffer with A/D converter in standard CMOS process. The buffer also uses a novel multi-path common mode feedback scheme to stabilize the common mode loop at high speeds. Another major problem in achieving very high Signal to Noise and Distortion Ratio (SNDR) is the capacitor mismatch in Digital to Analog Converters (DAC) inherent in the A/D converters. The mismatch between the capacitor causes harmonic distortion, which may not be acceptable. The analysis of Dynamic Element Matching (DEM) technique as applicable to broadband data-converters is presented and a novel second order notch-DEM is introduced. In this thesis we present a method to calibrate the DAC. We also show that a combination of digital error correction and dynamic element matching is optimal in terms of test time or calibration time. Even if we are using dynamic element matching techniques, it is still critical to get the best matching of unit elements possible in a given technology. The matching obtained may be limited either by random variations in the unit capacitor or by gradient effects. In this thesis we present layout techniques for capacitor arrays, and the matching results obtained in measurement from a test-chip are presented. Thus we present various design techniques for high speed and low noise A/D converters in this thesis. The techniques described are quite general and can be applied to most of the types of A/D converters.