ABSTRACT

DAC Linearization Techniques for Sigma-delta Modulators

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Digital-to-Analog Converters (DAC) form the feedback element in sigma-delta modulators. Any non-linearity in the DAC directly degrades the linearity of the modulator at low and medium frequencies. Hence, there is a need for designing highly linear DACs when used in high performance sigma-delta modulators. In this work, the impact of current mismatch on the linearity performance (IM3 and SQNR) of a 4-bit current steering DAC is analyzed. A selective calibration technique is proposed that is aimed at reducing the area occupancy of conventional linearization circuits. A statistical element selection algorithm for linearizing DACs is proposed. Current sources within the required accuracy are selected from a large set of current sources available. As compared with existing calibration techniques, this technique achieves higher accuracy and is more robust to variations in process and temperature. In contrast to existing data weighted averaging techniques, this technique does not degrade SNR performance of the ADC. A 5th order, 500 MS/s, 20 MHz sigma-delta modulator macro-model was used to test the linearity of the DAC.