500 MHz IF digitizer for software defined radio with digital calibration

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Abstract

This project deals with the design of ADC which can digitize IF signals in a radio receiver. The ADC architecture is a fourth order continuous time bandpass sigma-delta ADC running with a 500 MHz clock. A new OTA architecture with high linearity is used in the design of the gm-C bandpass filter with a center frequency of 125 MHz. A digital calibration scheme running on an external DSP is used to tune the center frequency and Q of the filter. The calibration scheme also corrects non-idealities arising from DAC.

Description

The block diagram of software defined radio architecture is shown in Fig. 1. The IF ADC is implemented as a fourth order continuous time bandpass ΣΔ ADC in TSMC 0.35 µm CMOS technology. The architecture has NRZ DAC waveform for reduced sensitivity to clock jitter. The bandpass filter is OTA-C filter with a linearized OTA for good distortion performance. The value of DAC currents are scaled for optimum power consumption and maximum SNR with good margin for stable operation. The architecture was verified first using Matlab/Simulink simulations and schematic/post-layout simulations were done in Cadence.

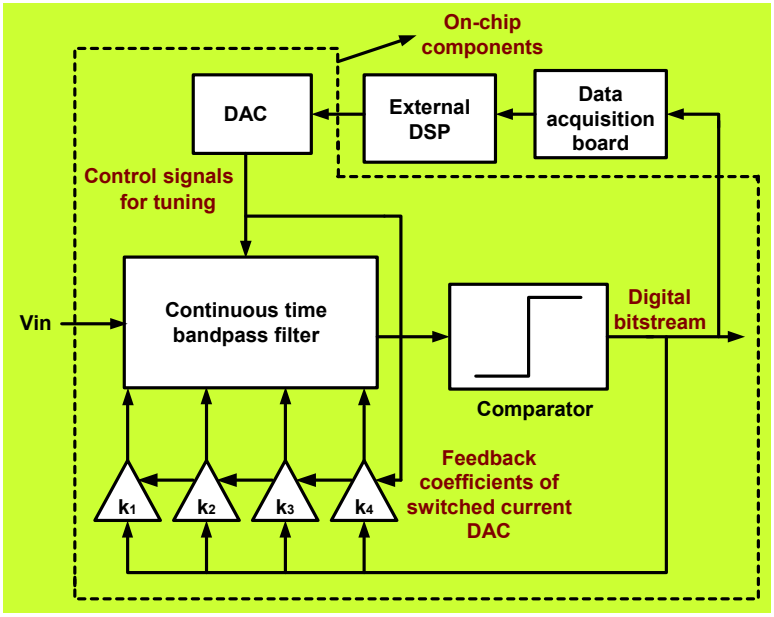

Fig 2 Block diagram of the tuning scheme

A tuning scheme is proposed to adjust the center frequency, and Q of filter, along with tuning of DAC currents for optimizing the SNR of the ADC over PVT variations. The block diagram of the tuning scheme is shown in Fig. 2. The center frequency and Q of the filter can be estimated by performing a Fast Fourier Transform (FFT) on the digital output bit stream. This property is used in the tuning scheme by capturing the bit stream

using an off-chip data acquisition board and then processing it using an external DSP. The errors in center frequency and Q are computed in the DSP and the error correction (tuning signals) is applied back to the filter and DAC currents using a DAC. The digital calibration scheme is shown in Fig 3. A test tone in applied in the loop at the comparator input. The loop first tunes for center frequency and then tunes the Q of the filter.

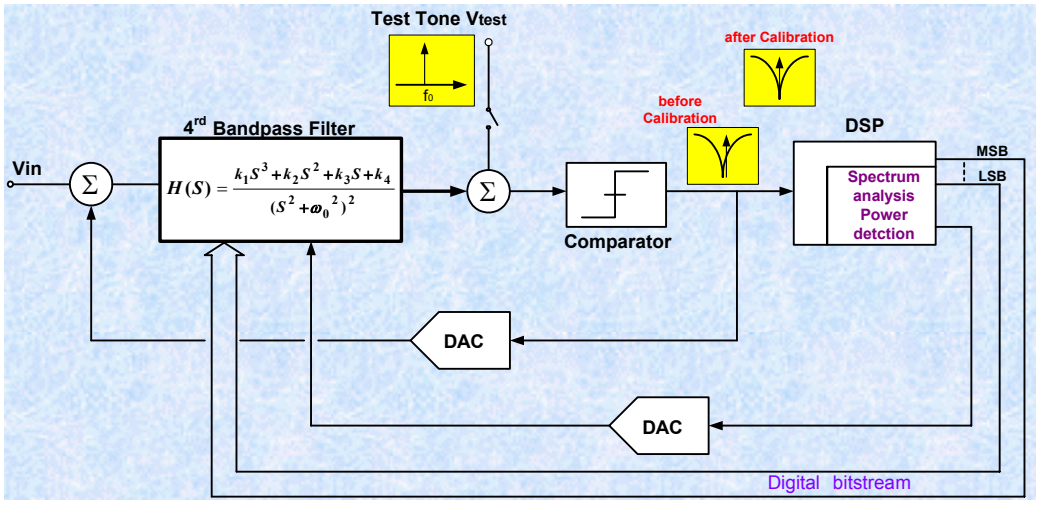

Fig 3 Digital calibration of the ADC

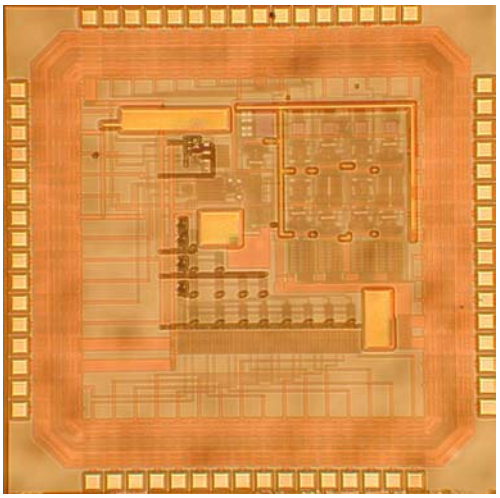

Fig 4 Microphotograph of the chip

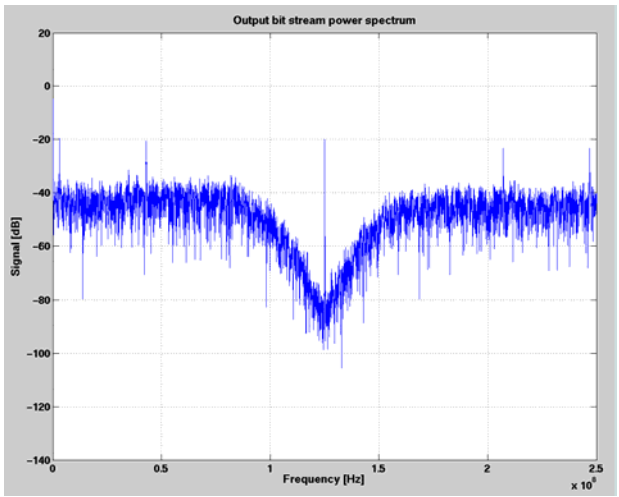

Fig. 4. post-layout simulation.

Status of project

The chip is currently under characterization