Low Power CMOS DTV Tuner Design

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Abstract: Low power CMOS DTV tuner is strongly needed for current DTV receiver. Conventional tuner solution is based on Bipolar or BiCMOS technology. Furthermore many off-chip components are necessary needed. In this project, we will try to implement a low power, SAW-less, CMOS DTV tuner. To demonstrate the idea, key blocks of tuner like VGA and mixer and frequency synthesizer is designed.

Description: The aim of this project is to design key blocks for off air ATSC digital television tuner. Conventional tuner designs use dual conversion architecture. First the channels are moved to high frequency like 1GHz and selected by off chip SAW filter. Then the selected channel will be downconvertered to standard IF frequency 44MHz. That costly architecture relaxes the image rejection filter requirement and make high image rejection ratio like 60dB possible. To keep such high image rejection ratio but with lower cost becomes the key point of current DTV tuner designs. In this project, we propose to design single step down conversion tuner with double quadrature architecture. The quadrature signal of both RF input and LO drives are mixed with double quadrature mixer. After that a complex filter is used to filter out the image signal which is located at the negative intermediate frequency (-44 MHz). The whole system block diagram is shown in figure 1. In this system, input I/Q match for RF and LO were relaxed and 60dB image rejection ratio is expected.

The analog front end for DTV tuner including wideband low noise viable gain amplifier and double quadrature downconverter will be designed. Wideband low noise amplifier must operate properly for a bandwidth bandwidth close to 800MHz; we will also generate differential signal to be processed by the mixer. The downconverter is composed by a broadband RF I/Q generator and a double quadrature mixer and an IF stage image rejection polyphase filter. The broadband I/Q generator is implemented with passive polyphase filter and its attenuation in positive frequency will be at least 40dB. Differential input RF signal will create quadrature outputs with I/Q mismatch less than 3%. Four matched broadband mixers are implemented for double quadrature mixing operation. After that another passive polyphase filter will be used with over 60dB negative frequency attenuation.

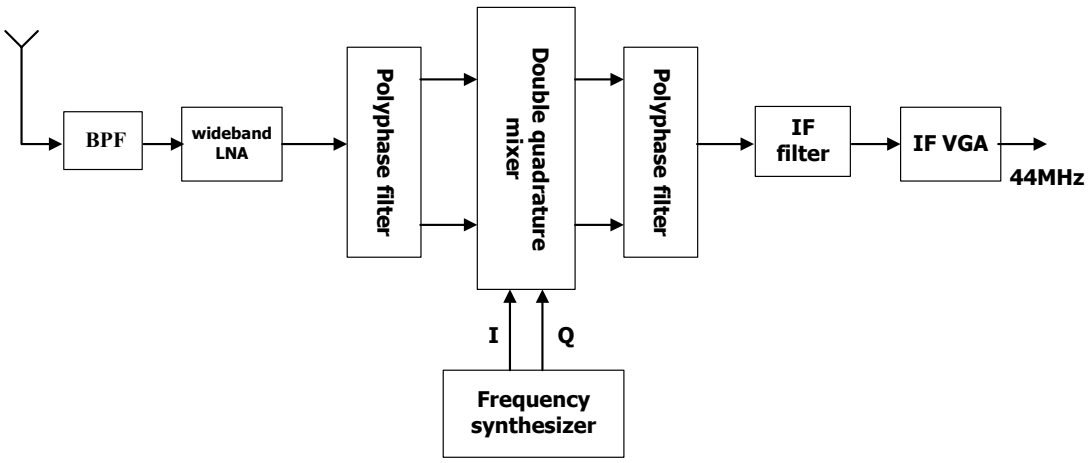

Fig.1 single step down-conversion DTV tuner design

The frequency synthesizer is also designed here to supply LO drive and the frequency range covers from 98MHz to 850MHz. To have good channel selection, high phase noise requirement like -80dBc at 10 kHz offset is necessarily needed. To have such wide range and good phase noise, 4 LC VCO are used and phase locked loop (PLL) will help to have better phase performance.

Status: These key blocks have been fabricated with TSMC 0.35um technology. Layout was shown above on figure 2. We expect to get image rejection ratio around 50dB cover all of frequency band for the whole RF front-end. Also we hope we can have 8dB NF and enough linearity like 5dBm IIP3.

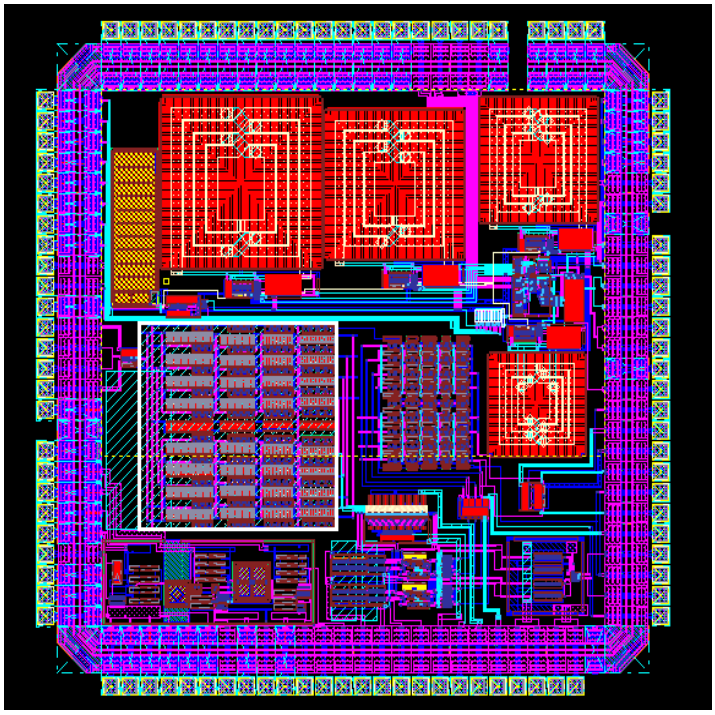

Fig.2 CMOS DTV Tuner Key Blocks Layout