10Gb/s Clock and Data Recovery System
# for SONET OC-192 Standard

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Abstract

This project is a clock and data recovery (CDR) chip working at 10Gb/s for SONET OC-192 application. The CDR will work as the analog front-end in a SONET optical receiver. This chip features a novel referenceless dual-loop architecture, which includes a linear frequency-locking loop and a quadri-level phase-locking loop. This architecture will enable us to achieve both fast locking speed and small jitter when the CDR is locked. The CDR is based on a half-rate 4-stage LC oscillator at 5GHz with quadrature output signal.

Description

We are designing a clock and data recovery (CDR) chip working at 10Gb/s based on SONET OC-192 standard. The CDR is to be used as the most critical module in the optical receiver for OC-192 standard. The entire diagram of a SONET receiver is given below,
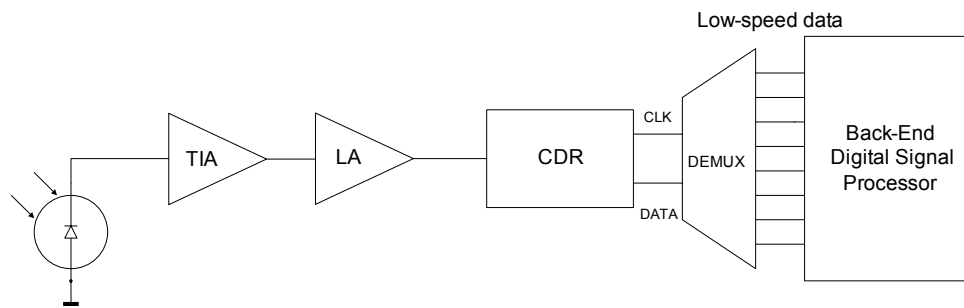
The photo-sensitive diode picks up the optical signal and converts it into weak current signal. The trans-impedance amplifier (TIA) converts the current signal into amplified voltage signal. The limiting amplifier further amplifies the voltage signal until maximum amplitude is reached, typically around 250 mV. The clock and data recovery block (CDR) recovers both data and clock signal from the incoming 10Gb/s data stream. The recovered data is then demultiplexed into multiple low-speed data streams, which is processed by the back-end digital-signal processor at the final stage.

For CDR's using dual-loop structures, some of them need a reference clock signal while others don't need any reference signal. We choose the referenceless implementation because it can save cost and increase the level of integration. In clock & data recovery systems, both frequency detectors and phase detectors can be either linear or binary. Linear detectors produce output signal linearly related to input phase/frequency difference. Binary detectors produce output signal only related to the sign of the input phase/frequency difference. We use linear frequency detector in the frequency-locking loop to achieve large capture range and use binary phase detector in the phase locking loop to ensure minimum jitter and phase noise in locked mode. Conventional binary phase detectors have only two output levels. We use a quadri-level phase detector to achieve both fast locking and minimum phase noise.

The block diagram of the entire CDR is given below,
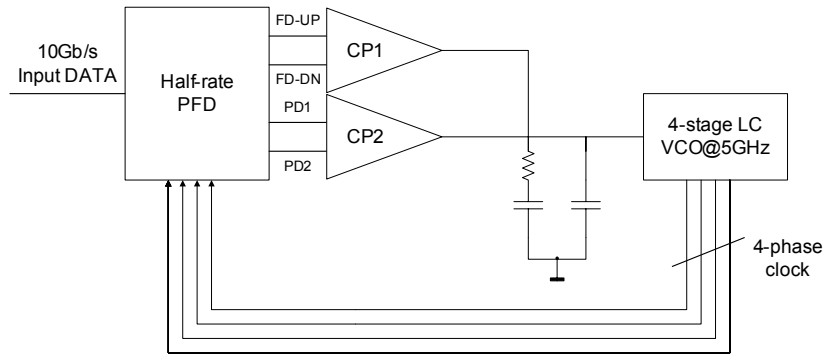
The CDR works on a half-rate basis, i.e., the oscillation frequency of the VCO is only half of the input data rate. That avoids the design of a 10GHz VCO which is very hard to implement in 0.18um CMOS processing and burns a lot of power. The phase and frequency detector also works on a half-rate basis, comparing the phase and frequency difference between 10Gb/s input data and 5Gb/s clock. Due to the fact that we use a referenceless half rate PFD, 4-phase clocks are needed by the PFD to produce correct phase and frequency difference signals. The 4 differential clock signals are 45 degrees apart from each other.

A screenshot of the chip layout is given below,
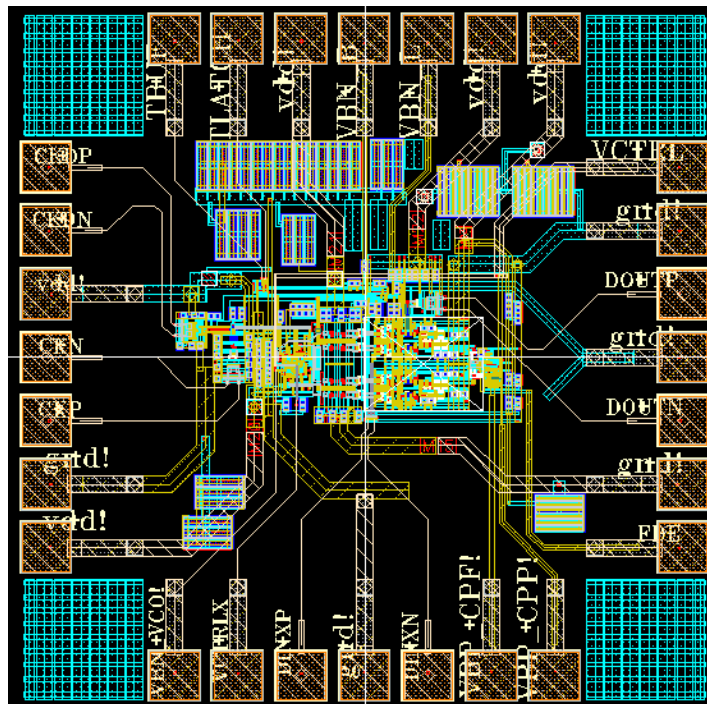
Status
The chip is under fabrication.