SC Oscillator with Improved Linearity

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Abstract.
The goal of this research is to improve the linearity of integrated oscillator based on switched-capacitor band-pass filter with a low Q-factor in order to achieve a feasible integration. With the minimum addition control digital control circuit, high linearity can be achieved by suppressing 3rd harmonic which requires high Q of filter in traditional way.

Description.
The aim of this research is to increase the linearity of oscillator based on BPF (band-pass filter). Advantage of BPF based oscillator is that the oscillation amplitude is effectively controlled by non-linear block (limiter) and it is easy to make oscillator stable. Disadvantage is that the linearity of oscillator is heavily dependent of Q of BPF and very high Q is required for BPF in order to have high linearity for oscillator. For SC (switched-capacitor) BPF, high capacitor spread is needed to achieve high Q of BPF, which consumes large chip area.

In this research, new type of SC oscillator based on SC BPF has been proposed and high-linear output can be achieved without high Q of BPF. Instead of increasing Q of BPF, by rejecting harmonics of input of BPF, linearity of oscillator can be much improved and ideally independent of Q of BPF. The proposed SC oscillator includes a conventional SC oscillator and an additional digital control block which generates control signals with respect to master clock and they are used in BPF to switch an additional SC branch and, the signal through this branch is combined with square wave from limiter. In the proposed technique, by minimizing the effects of the 3^{rd} and 5^{th} order harmonics, the overall THD has improved. The additional digital control block can be implemented with a number of flip-flops which consume small area and power. This harmonic rejection can be effectively done in SC circuit since it has a master clock and voltage adder inherently. Figure 1 and figure2 show the block diagram for conventional and proposed SC oscillators. The digital control block has an input from the limiter and generates control signal to BPF.

In order to demonstrate the improvement of linearity through harmonic rejection, oscillator based on SC BPF was designed in TSMC 0.35um CMOS process. The designed circuit has a 10.7MHz for a center frequency, 85.6MHz for clock frequency and 10 for Q of BPF. Figure 3 shows the full chip design and it was submitted to MOSIS and it's on fabrication.

Status of the project.
Chip was designed and submitted to be fabricated
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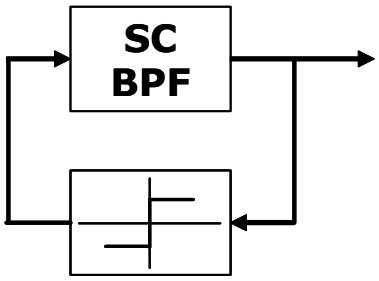

Fig. 1 Conventional SC oscillator

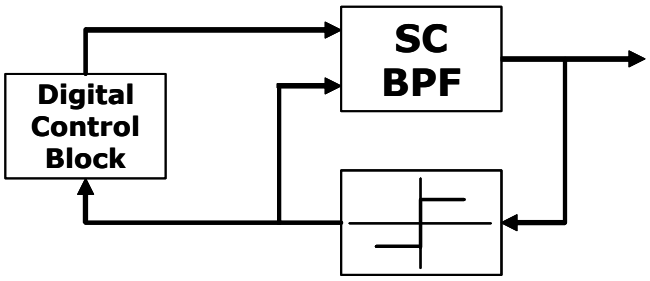

Fig. 2 Proposed SC oscillator

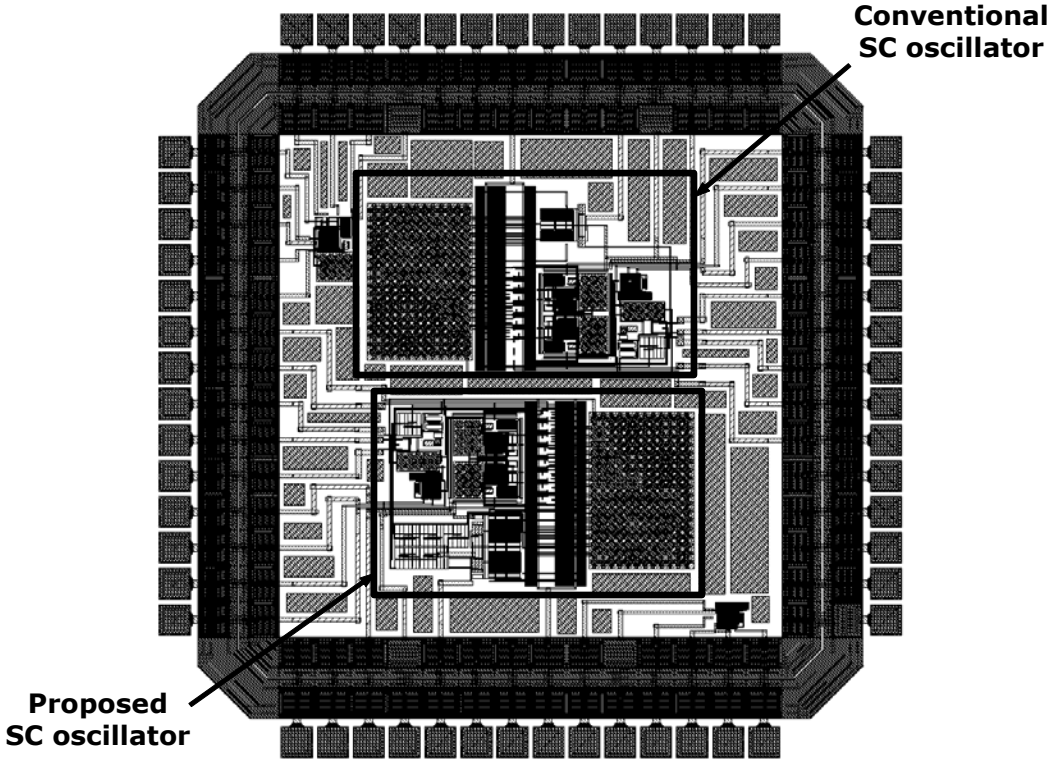

Fig. 3 Layout of SC oscillator