Capacitor-less Low Dropout Voltage Regulator with Fast Transient Response

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Abstract

The study of power management techniques has increased drastically within the last few years corresponding to the vast increase in the use of portable, handheld battery applications. These power management systems typically contain several LDO voltage regulators that require large external capacitors. The large external capacitors can not be fully integrated in standard CMOS technologies and hinder the use of System-on-Chip (SoC) solutions. The capacitor-less LDO research sought to eliminate the large external capacitor. This posed several major design challenges: transient response degradation and stability. These obstacles were overcome with the use of a fast transient path which also served as the compensation mechanism. The proposed design technique showed promising results for both stability and transient response. The capacitor-less LDO regulator technique is currently being verified in a TSMC 0.35µm CMOS technology.

Description

The characteristics of a conventional LDO voltage regulator suffer significantly with the removal of the large external capacitor, typically a few microfarads. The design and compensation must also change. The figure below shows the pole location and movement for a conventional LDO regulator and for the capacitor-less LDO voltage regulator.

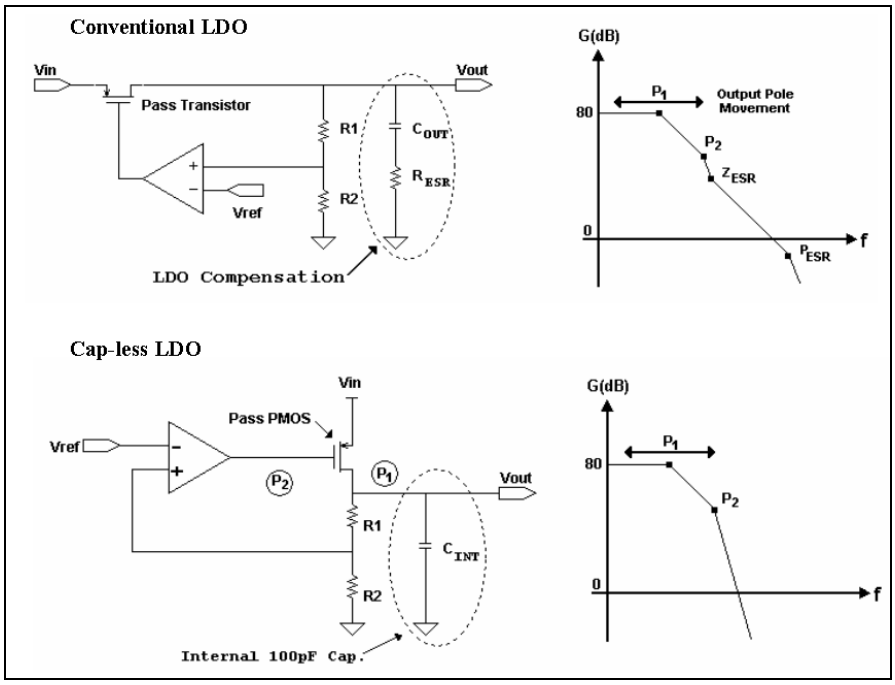

Figure 1. Comparison of pole locations for capacitor-less and conventional LDO regulators

The dominant pole, P_1, of the conventional LDO regulator depends on the output impedance and moves drastically with varying load current. Large load currents proves to be the most destabilizing condition for the conventional LDO, when P_1 moves close to P_{ESR}. The opposite

condition occurs for the capacitor-less LDO where the no-load condition pushes the load-dependent pole, P_1, in close proximity to the error amplifier pole P_2.

The current research solved this problem using multiple feedback loops. A dominant pole is generated internally, eliminating the load-dependent dominant pole and creating a relatively constant gain-bandwidth product. The basic structure is shown in Figure 2. The main loop creates the dominant pole and determines the gain-bandwidth of the overall system. The error amplifier sees a low frequency pole looking into the compensation network, but the fast transient path is immune to this low frequency pole. The output pole and the internal compensation pole are clumped together and pushed out to high-frequency complex poles. This makes the capacitor-less LDO's GBW independent from load current variations.

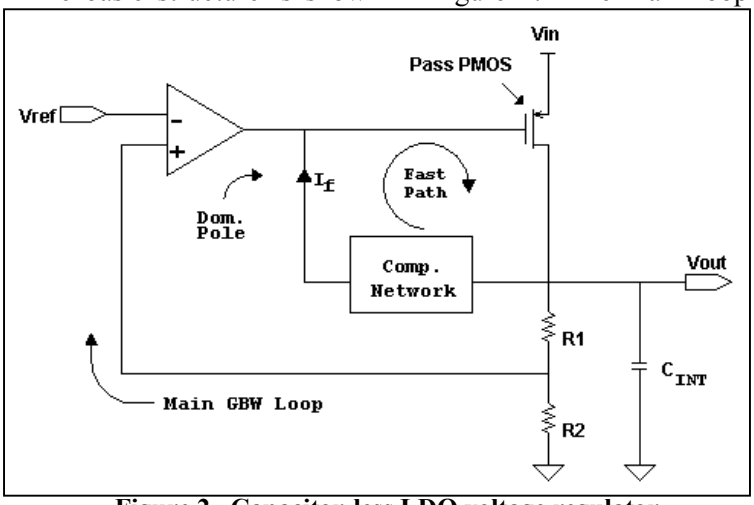

Figure 2. Capacitor-less LDO voltage regulator

The simulations proved that the compensation network along with the fast transient path stabilized the capacitor-less LDO voltage regulator. Figure 3 shows a transient simulation with and without compensation for a 50mA capacitor-less LDO regulator. Clearly, the fast transient path improves the load transient response as well as the regulator stability. The capacitor-less LDO, in current fabrication, has the preliminary specifications given in the table below.

LDO Specifications	
I_{MAX}	50mA
V_{DROP}	200mV
V_{OUT}	2.8V
GBW	700 kHz
I_{GND}	60µA
Noise	54µV
Turn-on t_S	<6µs
Full-Load Transient	<200mV

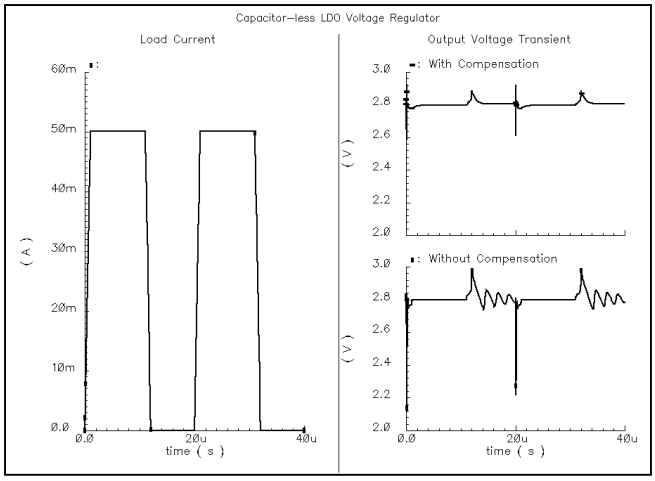

Figure 3. Capacitor-less LDO transient response

Status

The capacitor-less LDO voltage regulator with fast transient path is currently in fabrication in the TSMC 0.35um CMOS technology.