A Low-Voltage, Low-Power, High Sampling/Resolution Switched-Capacitor Pipeline ADC

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Abstract

This work attempts to provide a high sampling/resolution switched-capacitor (SC) pipeline A/D converter solution to match the demanding decrease in voltage supplies and power requirements for CMOS System-on-Chip (SoC) applications.

Description

With shrinking voltage supplies down to less than 1V, and current (power) consumption reducing for virtually all portable electronics to increase battery life, analog design is forced to comply. One of the major analog building blocks found is most System-on-Chip (SoC) solutions is the A/D Converter. For high sampling/resolution ADCs, the most popular architecture is the Pipeline ADC. However, with such limited design boundaries—voltage and power—and Pipeline ADC overall performance linked to that of its first stage OTA (OPAMP), one is forced to depart from the conventional techniques into new, and not quite established, design approaches such as Positive Feedback, Transconductance Enhancement/Multiplication, Threshold voltage shifts, Gain correction... etc. in an attempt to maintain the same performance of its predecessors when voltage supply and power consumption were of little concern.

Status

The specifications of the ADC are yet being finalized, with an expectation of 1V, 10-12b resolution, and 100-150Ms/s to be fabricated in either IBM 0.13 or TSMC 0.18 technologies. Also, prototypes of Amplifier topologies are being designed for fabrication during the summer of 2005.

Other Research Projects

- Low-Voltage, Low-Power ΣΔ Modulator for Audio Applications
- Positive Feedback Techniques
- High Frequency LC Filters