A CMOS RF RMS Detector for Built-in Testing of Wireless Transceivers

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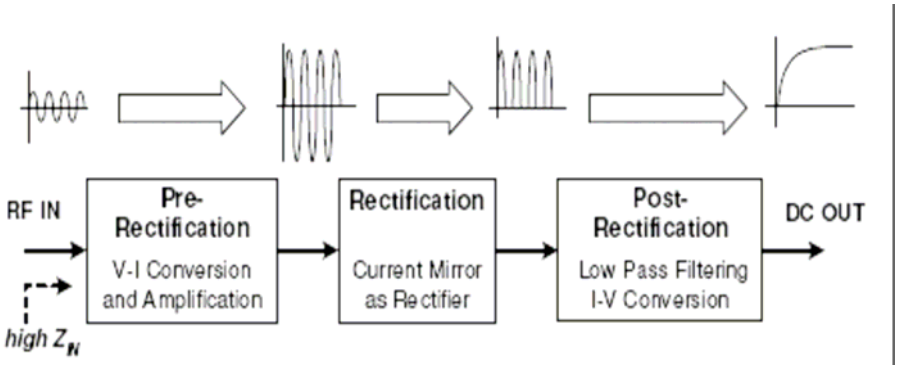
ABSTRACT: This project involves the design of a CMOS RF RMS Detector that converts the RMS voltage amplitude of an RF signal to a DC voltage. Its high input impedance and small area make it suitable for the built-in-testing of critical RF blocks of a transceiver such as a Low Noise Amplifier (LNA) and Power amplifier (PA) without affecting their performance and with minimum area overhead.

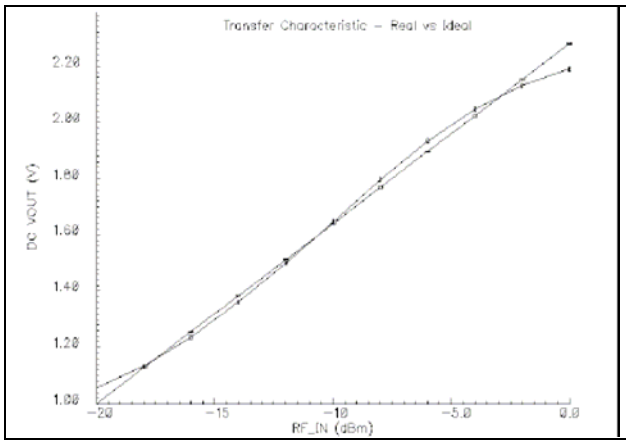
DESCRIPTION:

The need to accelerate the time-to-market by providing a fast fault diagnosis during the product development phase and to reduce the cost of testing for high-volume manufacturing necessitates the development of efficient testing techniques for RF systems and components. Further, the characterization of the individual building blocks is desirable to detect parametric faults, improve the fault coverage and accelerate the product development phase. Towards this end, Built-in-Self-Test (BIST) techniques are very useful.

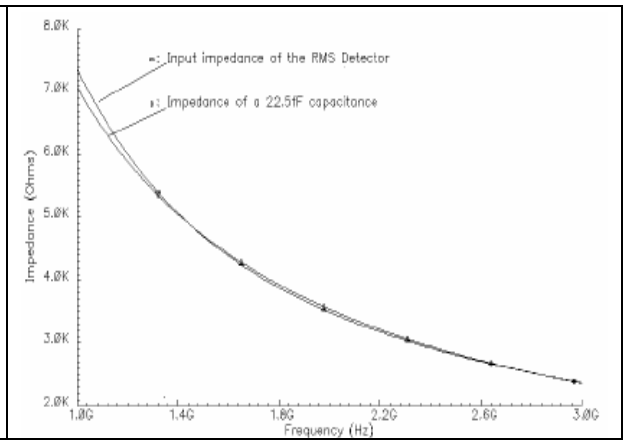
This project tackles the challenge of designing a full-CMOS implementation of the RMS detector for RF frequencies. It consists of three main stages:



The target frequency of operation for this design is 2.4 GHz, since this is the ISM band employed by widely used wireless standards such as Bluetooth, Wi-Fi and Zigbee. The following picture shows the input-output characteristic of the RMS detector and its input impedance as a function of operating frequency:



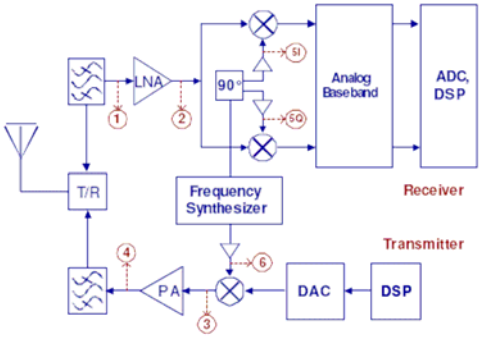
TRANSFER CHARACTERISTIC

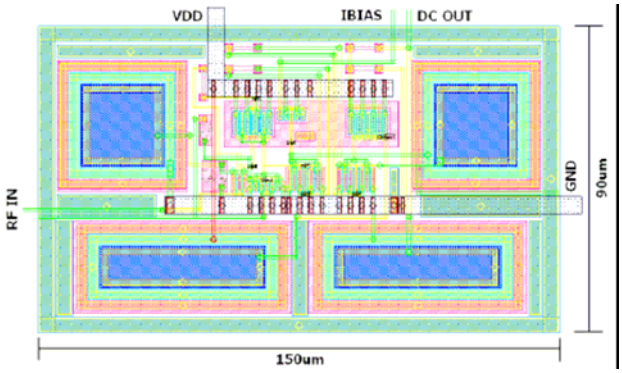


INPUT IMPEDANCE

TRANSCEIVER TESTING THROUGH ON-CHIP RMS DETECTION:

A typical transceiver with possible test points is shown below:





On-chip RMS detector connected at various strategic test points as shown above can enable functional verification of the RF blocks in the system using a low-cost-tester and/or analog-to-digital conversion and digital processing circuitry available on-chip. Multiple nodes can be observed from a single output pad since DC voltages can be easily multiplexed. The main performance metrics such as gain, output power and 1-dB compression pint can be tested with reasonable accuracy by measuring DC voltages.

The following table summarizes the performance achieved so far:

Technology	TSMC 0.35µm
Area	0.0135mm^2
Gain	60mV/dBm
Linear Dynamic Range	20dB
Supply Voltage	3.3 V
Power Consumption	10mW
Settling time	<40ns

STATUS:

An attempt is being made to test a Low Noise Amplifier at 2.4 GHz for its power gain and 1-dB compression point using the RMS detector in CMOS 0.35 μm technology.