A Frequency Synthesizer for Wireless LAN 802.11a and 802.11b Multi-Standard Transceiver

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Abstract

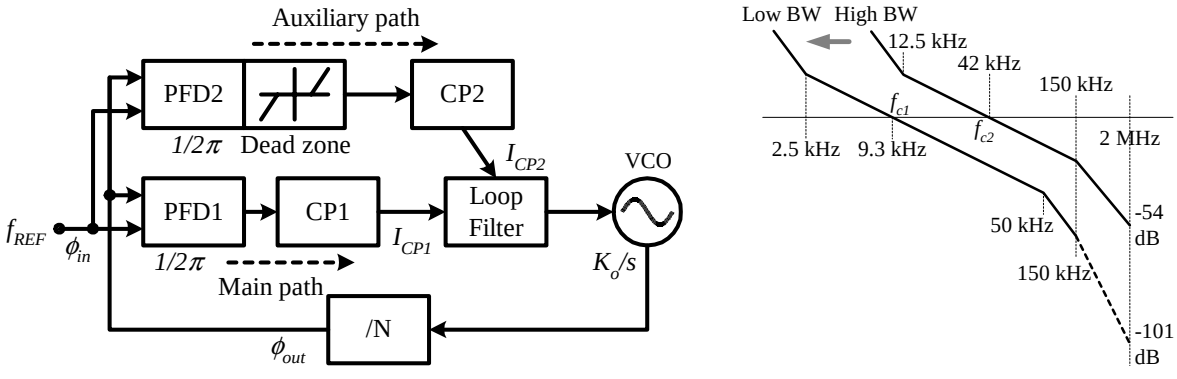
A BiCMOS frequency synthesizer compliant for both Wireless LAN (WLAN) 802.11a and 802.11b standards is presented. Proposed adaptive dual-loop PLL architecture improves reference spur rejection and settling time performance. The synthesizer is fabricated in a 0.25 μm BiCMOS process and dissipates 70 mW from a single 2.5 V supply. It occupies a silicon area of 1.7 mm^2. Test-chip measurement results show -56 dBc reference spurs at a frequency offset of 2 MHz, while maintaining a settling time close to 80 μs.

Description

1. System Architecture

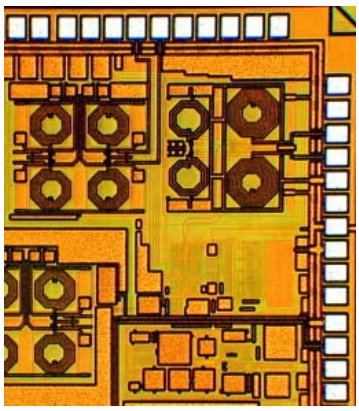
Narrow loop bandwidth is particulary useful to reject reference spurs. System level simulation results show that the reference spur must be at least 36 dB below the carrier signal to keep a BER better than 10^{-5} when the input SNR is 11.5 dB. However, if the bandwidth is too narrow, the loop time constant becomes too slow to meet the settling time requirement.

The problem of slow settling time can be avoided by utilizing the adaptive dual-loop PLL (ADPLL) as a speedup method. The fundamental idea of the adaptive dual-loop PLL is shown in Fig. 1. When the loop is stable, and thus the phase error small, only the main loop is active and the synthesizer operates with a narrow loop bandwidth. When the phase error becomes large due to a frequency step in the feedback path, the auxiliary path becomes active and pushes the loop bandwidth to a higher frequency. Once the output signal is close enough to the target frequency, the loop bandwidth returns to its original value so that any spurious signal is rejected. Fig. 1(b) shows the actual locations of poles and zeros for this implementation. Loop bandwidth is kept narrow at 9.3 kHz during the steady state and is pushed to 42 kHz for faster settling during the transition state.



(a) (b)

Figure 1: (a) ADPLL architecture (b) Transition of transfer function



(a)

(b)

Figure 2: (a) Chip microphotograph (b) Settling time measurements

Table 1: Measurement results summary

	802.11a	802.11b
Tuning range	$5180 \sim 5805$ MHz	$2412 \sim 2472$ MHz
Spurs	-56 dBc at 2.5 MHz	-59 dBc at 2 MHz
Settling time	$\simeq 80$ μs	< 80 μs
Phase noise	$-141 \sim -136$ dBc/Hz at 40 MHz offset	$-143 \sim -140$ dBc/Hz at 25 MHz offset

The increased spur rejection is obtained through a considerable reduction of loop loop bandwidth on the main path. In order to reduce the loop bandwidth substantially, very large capacitors may be required. Thus the direct application of an ADPLL may not be a practical solution for spur rejection. To overcome this problem without a considerable penalty in silicon area, an active capacitor multiplier is introduced to implement large capacitors.

2. Measurement Results

The proposed synthesizer was fabricated through MOSIS in a 0.25-μm BiCMOS process. Fig. 2(a) shows the microphotograph of the fabricated chip. The synthesizer dissipates 70 mW from a single 2.5 V supply including all the biasing circuits on the PCB, and occupies a chip area of 1.7 mm^2. An effective capacitance of 975 pF is implemented with the active capacitance multiplier occupying only 0.06 mm^2 of die area with minimal overhead on power consumption; the bias current needed for the capacitance multiplier is 10 μA. Fig. 2(b) shows a settling time of about 80 μs. The figure also shows that the settling time is increased to about 250 μs when the wide bandwidth loop is disabled. The rest of the measurement results are summarized in Table 1.

Status

The result is submitted to the IEEE Journal of Solid-State Circuits.