

# A LOW POWER, 350MHz, 24dB PROGRAMMABLE BOOST FILTER FOR READ CHANNEL APPLICATIONS

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## ABSTRACT:

High frequency Boost is commonly incorporated in continuous time filter to provide equalization for the read channel. This design focuses on deriving a power efficient architecture and circuit techniques for realizing large boost for high frequency continuous time filters. The other specifications of the filter include dynamic range of 36dB and SNR of 40dB over the signal bandwidth of 350MHz.

## DESCRIPTION:

High data rate Hard-Disk read write channels require low pass filtering before digitization. Also high frequency boost is embedded in the filter to achieve ‘pulse-slimming’ to reduce inter-symbol interference.

For achieving large boost gain, all the past approaches use feedforward or differentiator based architectures. The former approach suffers from voltage swing problem; an inevitable consequence of low frequency signal cancellation. It takes a lot of power to alleviate this problem using buffers. The latter approach is feasible only for low bandwidth and moderate (about 12dB) boost; the parasitic pole present in the differentiator needs to be pushed to high frequency at the expense of additional power. As a part of this research a ‘Power-Efficient Boost Architecture’ is proposed. To further enhance power efficiency, complementary transconductors and constant parasitic approaches are used. Also proposed is a power-efficient CMFB scheme for high frequency.

Post layout simulation results show that all the performance specifications are achieved with a bias current of mere 13mA. All previously reported solutions use more power for less bandwidth and smaller boost gain. Figure of merit in terms of MHz per mW per pole is about 3 times better than the best of previously reported solutions.

Figure 1 shows the layout of the prototype that has been sent for fabrication. And figure 2 show the boosted LP filter response. The filter has been designed using TSMC 0.35 um technology and has been submitted for fabrication. Characterization plan includes verification of boost gain, AC response of the filter, characterizing its linearity and PSRR.

**STATUS:** Chip is under fabrication.

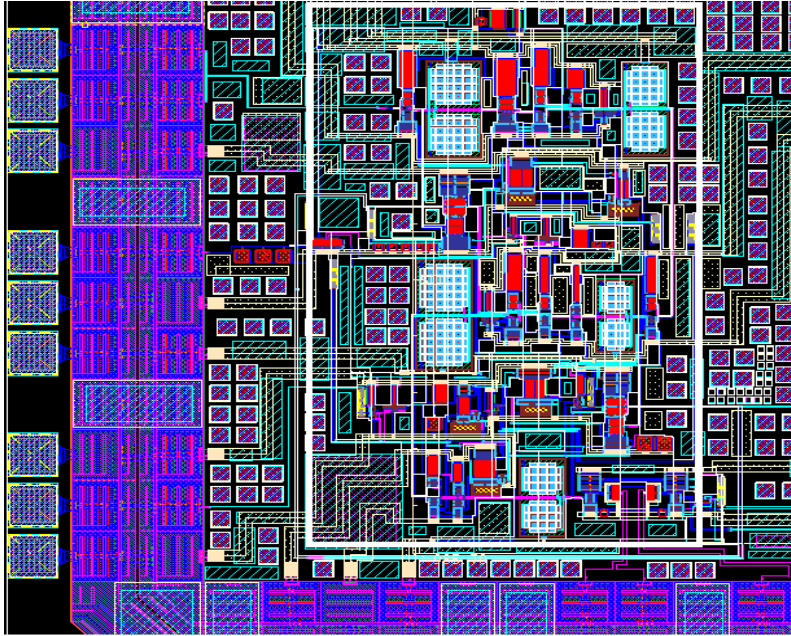


Figure 1 Layout of the prototype submitted for fabrication

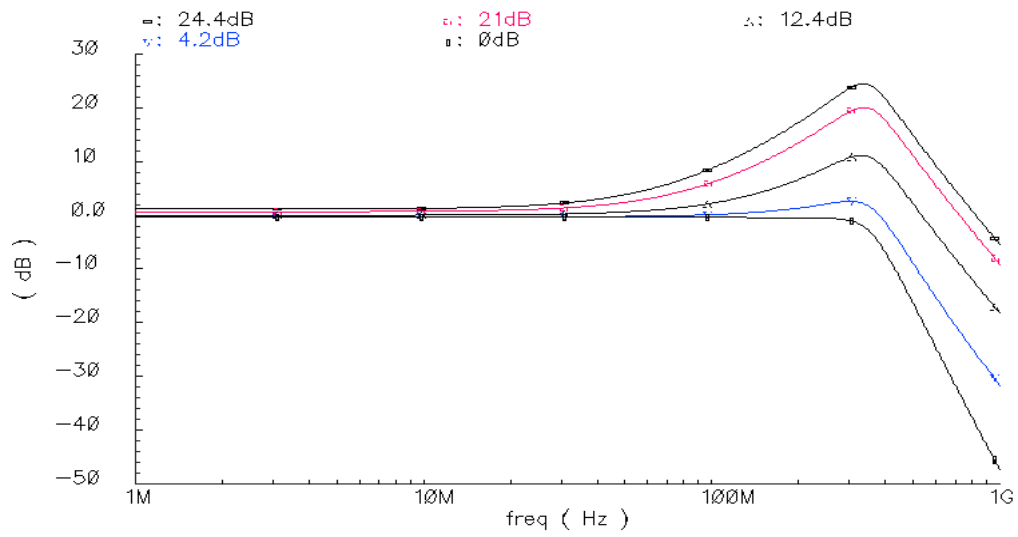


Figure 2: AC response of the filter depicting 24dB boost