A Low-Power High Dynamic-Range Broadband VGA for UWB Receiver

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Abstract
A CMOS Variable Gain Amplifier (VGA) is proposed for high frequency and low power broadband communication systems, such as Ultra-Wide Band (UWB) receiver. The VGA consists of a P/NMOS complimentary differential-pair with source degeneration, a high-swing current mirror stage with capacitive feedforward frequency compensation, and resistive load.

Description
Based on an OFDM UWB receiver system’s specifications, a VGA is needed in the baseband circuits between filter and ADC, to adjust the output signals from the filter to the required input signal level of the ADC, providing the largest signal-to-noise ratio to the ADC stage; hence the overall dynamic range of the receiver improves.

The major design challenges compared to the state of art VGA designs in the literature, are low power, high frequency operation, linearity and linear phase requirements.

a) To improve linearity and power-gain (transconductance) efficiency, a P/NMOS complimentary differential-pair with source degeneration input stage is used.

b) To achieve high bandwidth, the VGA is implemented with current-mode amplification using a high-swing current by simply change the source voltage of the input-side of the current mirror to obtain different current gain factors. Our study shows the proposed current mirror increases -3dB frequency up to 20% than that of a normal current mirror.

c) To further increase the bandwidth, differential capacitive feedforward frequency compensation was implemented to increase the bandwidth by more than 25%. A common-mode offset cancellation is implemented at the output stage to fix the output DC level.

d) The VGA is digitally programmable from 0-42 dB with steps of 2 dB.

A layout view of the VGA is shown in Figure 1, and a comparison of the-state-of-the-art VGA designs in the literature is listed in Table 1.

Status
Chip was sent for fabrication, and will be fully characterized in June ~ July, 2005.
Table 1. Performance Comparison with the State of the Art VGA Designs in the Literature

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Tech</th>
<th>Gain (dB)</th>
<th>BW (MHz)</th>
<th>Linearity</th>
<th>Noise</th>
<th>Power (mW)</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>0.25um CMOS</td>
<td>Up to 35</td>
<td>300</td>
<td>THD: -62dB</td>
<td>NF: 8.6dB@Av=35dB</td>
<td>132 (3V/40mA)</td>
<td>NA</td>
</tr>
<tr>
<td>[2]</td>
<td>0.18um CMOS</td>
<td>-42 ~ 42</td>
<td>350</td>
<td>IIP3: -22dBm@Av=42dB 0dBm@Av=0dB</td>
<td>NA</td>
<td>5.4 (1.8V/3mA)</td>
<td>0.185</td>
</tr>
<tr>
<td>[3]</td>
<td>0.35um CMOS</td>
<td>-65 ~ 35</td>
<td>430</td>
<td>IIP3: 8dBm@Av=30dB</td>
<td>NA</td>
<td>48 (3V/16mA)</td>
<td>0.48</td>
</tr>
<tr>
<td>[4]</td>
<td>0.35um CMOS</td>
<td>0 ~ 42</td>
<td>270</td>
<td>HD3: -55dB</td>
<td>NA</td>
<td>54 (2.7V/20mA)</td>
<td>0.15</td>
</tr>
<tr>
<td>Our Work</td>
<td>0.25um BiCMOS</td>
<td>0 ~ 42</td>
<td>400</td>
<td>IIP3: -10dBm@Av=42dB 20dBm@Av=0dB</td>
<td>NF: 13dB@Av=42dB 18dB@Av=0dB</td>
<td>9 (2.5V/3.6mA)</td>
<td>0.02</td>
</tr>
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</table>

Reference:

