A Low-Power High Dynamic-Range Broadband VGA for UWB Receiver

Lin Chen, José Silva-Martinez and Edgar Sánchez-Sinencio

Abstract
A CMOS Variable Gain Amplifier (VGA) is proposed for high frequency and low power broadband communication systems, such as Ultra-Wide Band (UWB) receiver. The VGA consists of a P/NMOS complimentary differential-pair with source degeneration, a high-swing current mirror stage with capacitive feedforward frequency compensation, and resistive load.

Description
Based on an OFDM UWB receiver system's specifications, a VGA is needed in the baseband circuits between filter and ADC, to adjust the output signals from the filter to the required input signal level of the ADC, providing the largest signal-to-noise ratio to the ADC stage; hence the overall dynamic range of the receiver improves.
The major design challenges compared to the state of art VGA designs in the literature, are low power, high frequency operation, linearity and linear phase requirements.

a) To improve linearity and power-gain (transconductance) efficiency, a P/NMOS complimentary differential-pair with source degeneration input stage is used.

b) To achieve high bandwidth, the VGA is implemented with current-mode amplification using a high-swing current by simply change the source voltage of the input-side of the current mirror to obtain different current gain factors. Our study shows the proposed current mirror increases -3dB frequency up to 20% than that of a normal current mirror.

c) To further increase the bandwidth, differential capacitive feedforward frequency compensation was implemented to increase the bandwidth by more than 25%. A common-mode offset cancellation is implemented at the output stage to fix the output DC level.

d) The VGA is digitally programmable from 0-42 dB with steps of 2 dB.

A layout view of the VGA is shown in Figure 1, and a comparison of the-state-of-the-art VGA designs in the literature is listed in Table 1.

Status
Chip was sent for fabrication, and will be fully characterized in June ~ July, 2005.

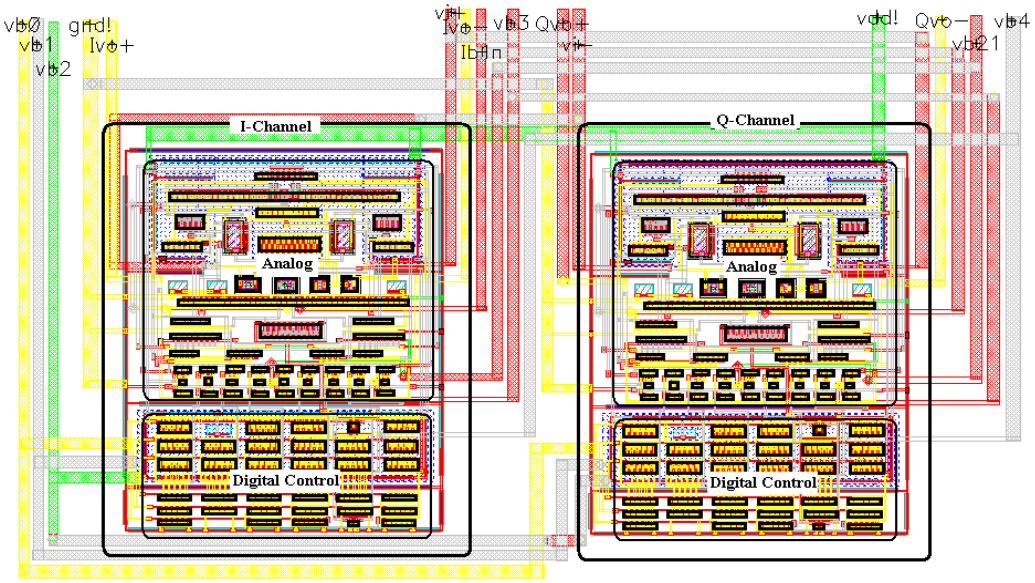

Figure 1. Layout View of the VGA

Table 1. Performance Comparison with the State of the Art VGA Designs in the Literature

Ref.	Tech	Gain (dB)	BW (MHz)	Linearity	Noise	Power (mW)	Area (mm^2)
[1]	0.25um CMOS	Up to 35	300	THD: -62dB	NF: 8.6dB@Av=35dB	132 (3V/40mA)	NA
[2]	0.18um CMOS	-42 ~ 42	350	IIP3: -22dBm@ Av=42dB 0dBm@Av=0dB	NA	5.4 (1.8V/3mA)	0.185
[3]	0.35um CMOS	-65 ~ 35	430	IIP3: 8dBm@Av=30dB	NA	48 (3V/16mA)	0.48
[4]	0.35um CMOS	0 ~ 42	270	HD3: -55dB	NA	54 (2.7V/20mA)	0.15
Our Work	0.25um BiCMOS	0 ~ 42	400	IIP3: -10dBm@Av=42dB 20dBm@Av=0dB	NF: 13dB@Av=42dB 18dB@Av=0dB	9 (2.5V/3.6mA)	0.02

Reference:

[1] Yonghua Tang and Randall L.Geiger, "A Highly Linear CMOS Amplifier for Variable Gain Amplifier Applications," Circuits and Systems, 2002 45th Midwest Symposium on, Volume: 1, 4-7 Aug. 2002

[2] J.K. Kwon, K.D. Kim, W.C. Song, and G.H. Cho, "Wideband High Dynamic Range CMOS Variable Gain Amplifier for Low Voltage and Low Power Wireless Applications," Electronics Letters, Vol. 39, May 15 2003

[3] Yong-Sik Youn, jang-Hong Choi, Min-Hyung Cho, Seon-Ho Han, and Mun-Yang Park, "A CMOS IF Transceiver with 90dB Liner Control VGA for IMT-2000 Application," VLSI Circuits, 2003. Digest of Technical Papers. 2003 Symposium on, 12-14 Jun. 2003

[4] Siang Tong Tan, and Jose Silva-Martinez, "A 270MHz, 1Vpk-pk, Low-Distortion Variable Gain Amplifier in 1 0.35um CMOS Process," Analog Integrated Circuits and Signal Processing, Vol. 38, Feb. 2004