2.5/10 Gigabit Bit/s Clock Data Recovery Circuit Techniques for Optical Communications

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Abstract

This research is focused on CMOS implementation of 2.5/10G Clock data recovery for OC-192 and OC-48 SONET applications using dual loop PLL based architecture. LC tank VCO is adopted in all research chips to achieve low phase noise. Linear Phase detector and binary phase detector architecture are researched and implemented in 0.35um and 0.18um CMOS technology. The circuit is optimized to meet SONET jitter tolerance and peaking standard.

Description

The volume of data transported over the telecommunications network make it necessary to develop data transceiver working at 10G Bit/S or above. Currently OC-192, running at approximately 9.95328 Gb/s, will be, or, are being deployed throughout North America, due to the rising response to the explosion in data traffic.

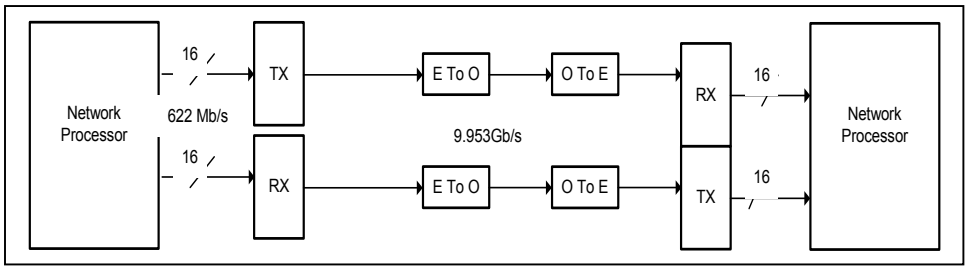

Fig 1 Sonet OC-192 Network Diagram

A network processor will convert input data into the form of 16 parallel signals, each operating at 622Mb/s. These signals are sent to the parallel inputs of the transmitter where they are synchronized to a precise reference clock and then serialized so that the output of the transmitter is a single channel operating at 9.95328Gb/s.The high speed serial transmitter output is used to modulate a laser driver, which generates the optical signal that is sent through a fiber. At the receiving side of the fiber, the light is applied to a photodiode connected to a transimpedance amplifier(TIA) which then converts the signal back to electronic form. The electronic signal is applied to a post-amplifier and then a limiting amplifier before it is applied to the receiver input. In the receiver a clock synchronized to the incoming data is generated using a clock data recovery (CDR) circuit. The recovered clock and re-timed data provided by the CDR are then applied to a demultiplexer which outputs 16 parallel signals, each at 622Mb/s. These signals are applied to another network processor which performs the necessary overhead and framing operations.

The primary objective of this project is to research the potential architecture for an integrated clock data recovery circuit with de-serializer operating at a clock frequency of 10 GHz for OC-192 optical communications. The main focus in this project is to use two loops for fast acquisition and large pull-in range of the phase locked loops. To overcome the ripple of the control line of the charge pump, a continuous-time mechanism is adopted to ease the glitches on the control line of the charge pump in the single-loop PLL. This method is robust in data recovery system and will be widely used in the future applications. Traditional CDR schemes use bipolar technology or GaAs BiCMOS technology, which are very expensive for commercial applications. In our proposed scheme, we use CMOS technology to construct the prototype chip, a lock detector and digital/analog phase detector will be used to monitor and sense the variation of the frequency and phase difference. This results in improved performance and less complex design challenge.

Status

The fabricated chips are shown in Fig 2 ,3 and 4. And one test result example is shown in the photo below. The measured phase noise is –107dBc @1MHz offset. Need optical tester to futher characterize the chips.Papaers are under preparation.

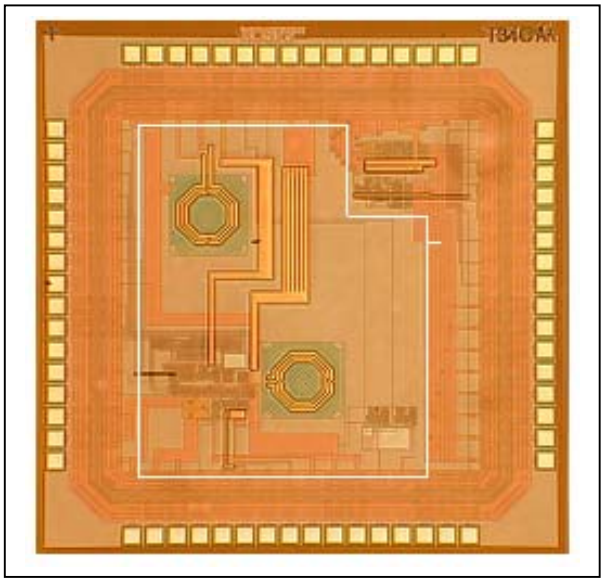

Fig. 2 Test chip for 2.5G CDR

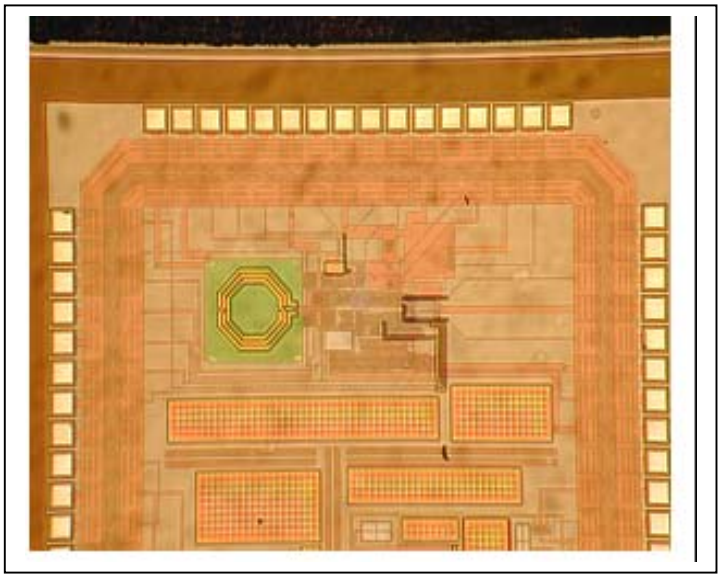

Fig. 3 Test chip for Half Rate 3.5G CDR

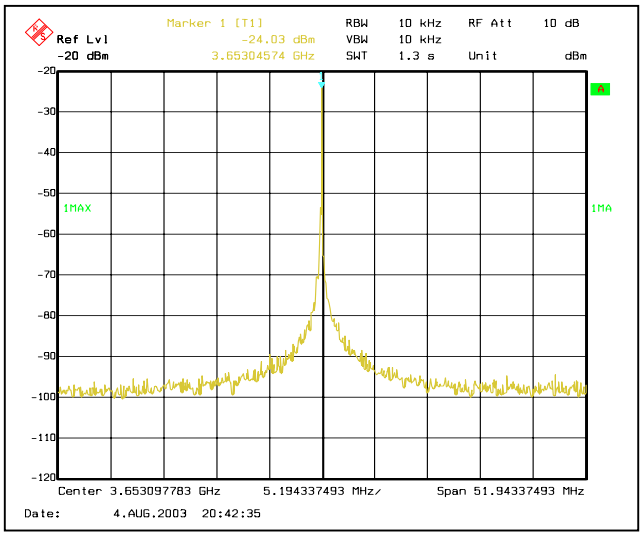

Fig.4 Frequency spectrum of the clock output of 3.5G CDR

Further research effort is spent on 10G CDR design. One more 10G CDR chip is fabricated at MOSIS and The chip photo is omitted at this time. Our characterization results show that it is possible to design Multi-Giga Herz Circuits using digital CMOS technology with satisfactory performance.