Wide-band high-resolution ΣΔ A/D converter

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Abstract

Wireless base station and VDSL transceiver require A/D converter with signal bandwidth more than 10MHz and resolution in the range of 12-14bits. Continuous-time ΣΔ A/D converter has the advantage of possible high signal bandwidth as well as low power consumption compared with discrete time counterpart. In this project, our target is to design a 12MHz-signal bandwidth continuous time ΣΔ A/D converter with resolution around 13 bits.

Description.

High-speed and high-resolution A/D converters are essential for high date-rate communication systems. For certain applications like wireless and VDSL transceiver systems, low power consumption is another very critical design constraint. Pipeline A/D converter is a conventional choice for the applications with ~25MS/s throughput and 12-14 bits resolution. However, the design of anti-aliasing filter for pipeline A/D converter could be a big challenge if the sample rate is only slight higher than Nyquist rate. ΣΔ A/D converter, on the other hand, has built-in anti-aliasing filter. Even if additional filtering is required, the oversampling of the modulator greatly ease the implementation of the filter. Compared with discrete-time ΣΔ A/D converters, continuous-time ΣΔ A/D converters have the advantage of high bandwidth and low power consumption. However, issues like clock jitter, RC time constant process variation and excess loop delay have to pay special attention for continuous-time ΣΔ A/D converters.

Although multi-loop (MASH) architectures ease the modulator stability problem, it needs very sophisticated signal process technique to deal with process variation and mismatches. For single-loop high order architecture, it's hard to synthesize a stable modulator with high resolution especially with low oversampling rate. For this project, a 4^{th} order single loop with 4-bit internal quantizer continuous-time ΣΔ A/D converter is proposed and synthesized. The target of this project is to achieve a signal bandwidth of 12MHz with around 13-bit resolution and minimal power consumption. All the critical issues like clock jitter sensitivity, process variation, mismatches and excess loop delay have been considered and addressed in system level design.

Status of the project

System level simulation is finished; circuit level design is on the way.