High-Speed Adaptive Equalizers for Serial Communications Systems

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Abstract

The objective of this work is the design of a high-speed transversal equalizer capable of operating at 1.25Gbps. Linear-phase active delay lines, a broadband analog FIR circuit, and a sub-sampled blind coefficient adaptation circuit are some of the innovations proposed in this work. The circuits are being designed in CMOS 0.35μm technology with ±1.5V supply.

Description

In broadband communications systems, the transmission of high-speed data is limited by the frequency response of the channel (twisted pair, coaxial line, fiber-optics or PCB traces). The limited bandwidth results in inter-symbol interference (ISI), which in turn may increase the bit error rate of such systems. To reduce the effect of ISI, adaptive equalizers are typically used. At data-rates below 100Mbps, equalizers are implemented as finite-impulse response (FIR) filters in digital signal processors (DSPs). As the data rates increase, DSPs can not process this high-speed data, and equalizers must be implemented in the analog domain. The challenge becomes on how to implement compact, low-power small-area FIR filters in the analog domain, particularly in CMOS technologies. Figure 1 shows the block diagram of an adaptive equalizer for 1.25Gbps (binary data) currently being designed in the Analog and Mixed Signal Center.

This fractionally-spaced-equalizer consists of a 5-tap FIR filter working at an equivalent sampling frequency of 2.5Gsamples/sec. Each active delay line is implemented with a linear-phase continuous-time filter. The multipliers are implemented with Gilbert cells, and their outputs are tied together into a high-speed summing node which also converts the output current into a voltage. The coefficients are optimized using a sub-sampled sgn-sgn LMS algorithm that does not require a training sequence. By running the adaptation circuit at a clock frequency 10 times slower than the symbol rate, this circuit consumes less power and has relaxed speed specifications that permit a compact implementation in CMOS technology.

Circuit simulations showing the eye diagram of a distorted binary stream prior and after equalization are shown in figure 2. The deterministic jitter for this particular example is reduced from 190ps to less than 57ps.

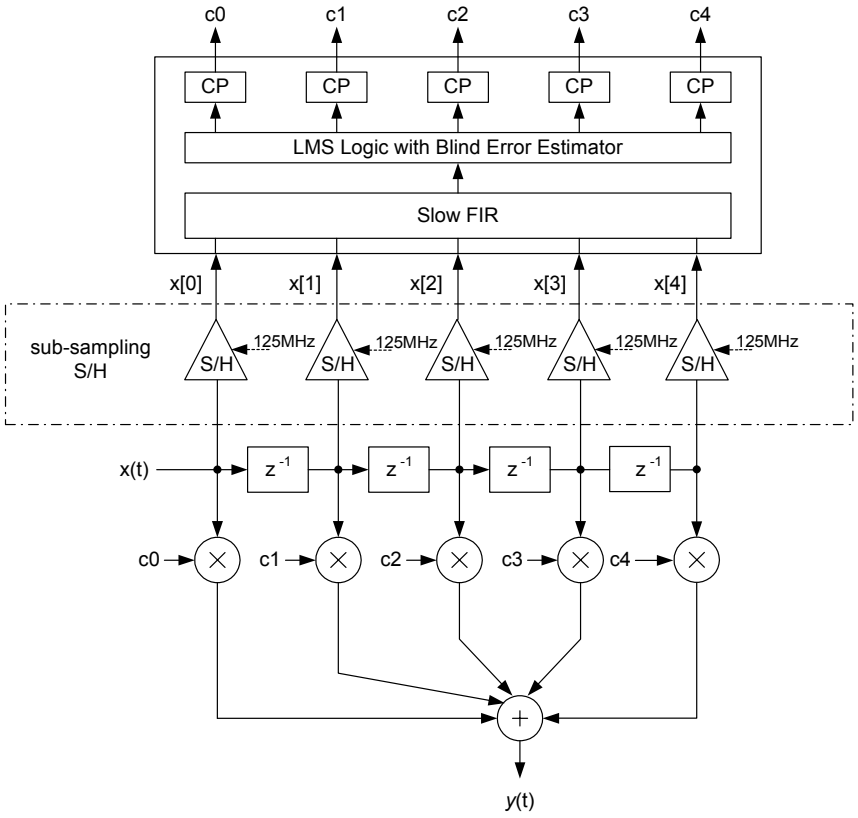
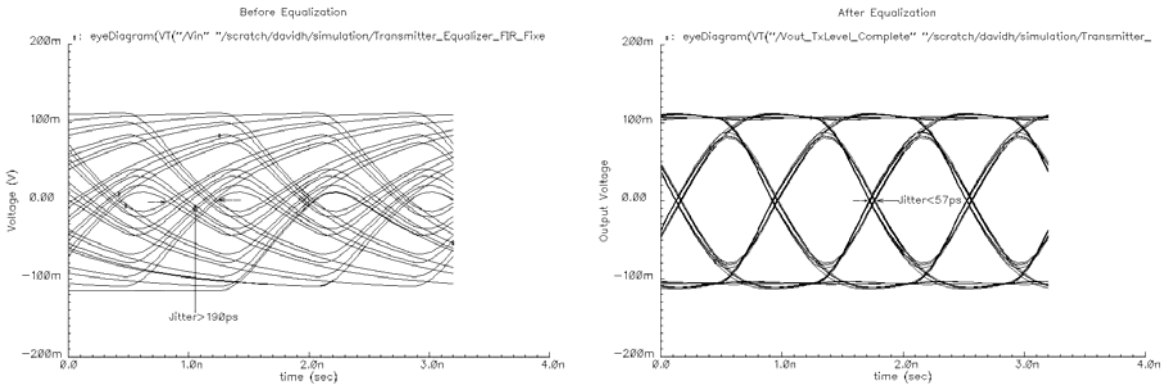


Figure 1. Block Diagram of the 1.25Gbps Adaptive Equalizer



(a) Before Equalization (b) After Equalization

Figure 2. Eye Diagram

Status

Final stage of circuit design and spice simulations.