

# Extremely Low Voltage Rail-to-Rail Operation for an Operational Amplifier with a Single PMOS Input Differential Pair

David Báez and Dr. José Silva-Martínez

## Abstract

A design approach for a quasi rail-to-rail input range operational amplifier is introduced. It uses a common-mode adapter to accommodate the common-mode component of the input signal to the amplifier input range. The adapter operates properly at 300 KHz and employs only 92  $\mu$ W. The amplifier is fabricated in an AMI 0.5  $\mu$ m process and achieves an IM3 of 48 dB at 300 KHz for an input signal of 0.8 Vpp. A 1 V total supply operation is used.

## Description

Modern VLSI circuits require lower power consumption and the use of lower supply voltages. It is necessary to develop new analog circuit topologies to perform adequately. The use of low voltage circuits with an input common-mode range that goes to both positive and negative supply rails is preferred to fully exploit the available voltage room, especially for buffer and sample and hold applications.

In this work the following approach is proposed. A common-mode adapter in a feedback loop controls the input common-mode component voltage of the operational amplifier enabling rail-to-rail input operation. The common-mode signal is obtained directly from the input stage of the operational amplifier, thus, no extra common-mode detector is required.

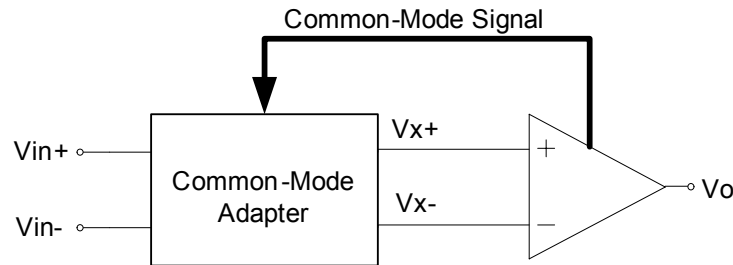


Fig. 1. Proposed Topology

In this work, an OTA composed by transistors MA1-MA2 amplify the error voltage. The reference voltage is selected as high as possible to minimize the power consumption due to the operation of the common-mode detector. The error voltage is converted into current by transistors MA3-MA4. These currents with the help of two resistances will shift the input common-mode DC level of the opamp to enable rail-to-rail operation of the amplifier.

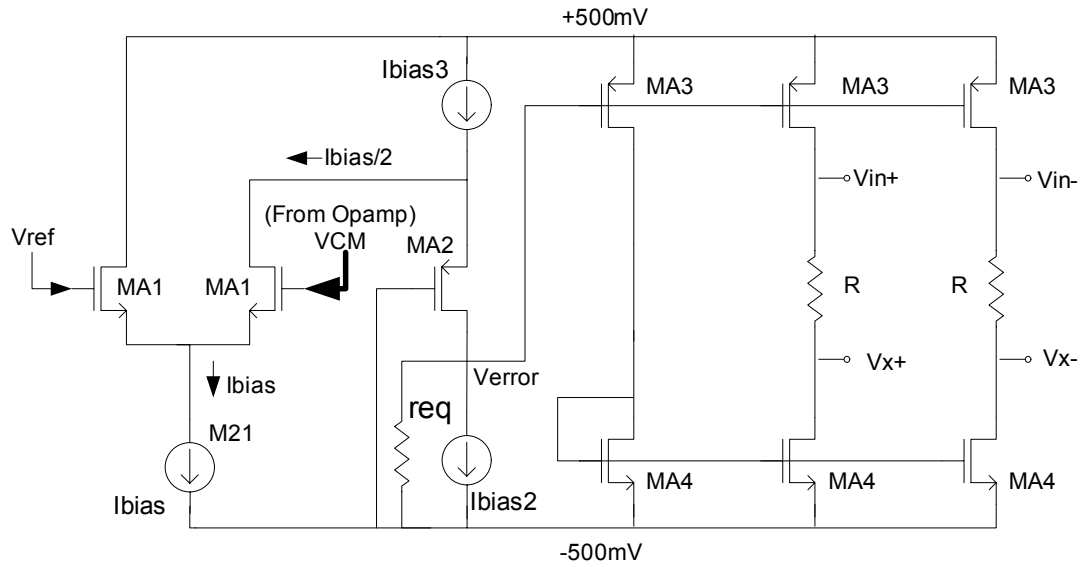


Fig. 2. Simplified Schematic of the Proposed Topology - Common-Mode Adapter

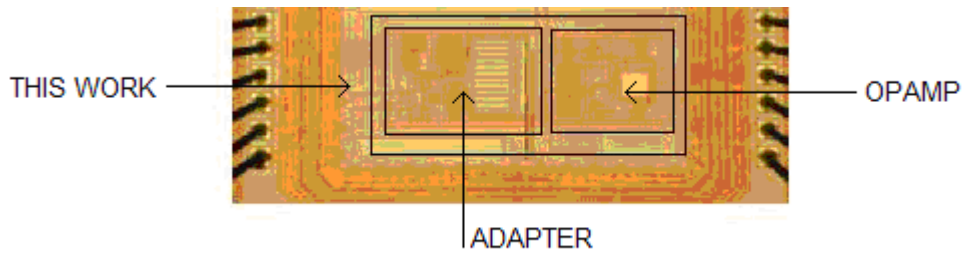


Fig. 3. Micrograph of the Proposed Topology

TABLE 1  
SUMMARY OF EXPERIMENTAL PERFORMANCE

Parameter	This Work
DC Gain	41.04 dB
PM	90°
IM3 at 0.8 Vpp, 100 KHz	48.95 dB
PSRR+	-57.5 dB
PSRR-	-48.31 dB

### Status

Chip has been characterized. Paper is under preparation.