3.8 Gs/s ADC with on-chip PLL for software radio

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Abstract
This project deals with design of analog to digital converters for software radio applications. Among various ADC architectures, continuous time bandpass (CTBP) sigma-delta ADC was found to be the best architecture for software radio applications. A new CTBP sigma-delta architecture with NRZ DAC is proposed for improved jitter performance. A complete on-chip solution with integrated PLL and ADC was designed in IBM 0.25 μm SiGe BiCMOS technology. Architecture and circuit optimization techniques are presented for low power operation.

Description
The block diagram of software radio architecture is shown in Fig 1. The ADC directly digitizes the RF input signal to a digital bitstream. Some advantages of software radio include multi-band support, easy re-configurability, easy addition of new standard etc. The RF ADC is implemented using a fourth order bandpass continuous time ΣΔADC. The design has an on-chip clock generation PLL which clocks the single-bit comparator at 3.8 GHz and the whole system is implemented using IBM 0.25μm SiGe BiCMOS technology. The architecture uses NRZ DAC waveform to mitigate aperture jitter effects and has a 950 MHz center frequency continuous time LC filter.
Previous architectures used RZ/HRZ DAC combination because there aren't enough injection points in a LC filter to realize the required loop transfer function. We propose a new NRZ architecture to implement the required loop transfer function. The concept of hard clipping and soft clipping was observed at integrator outputs by varying the DC gain of the integrators. Lossy integrators are a good solution to obtain stability with negligible reduction in the SNR of the ADC. On-chip PLL was used to generate clock of 3.8 GHz with very low jitter performance (< 1ps rms clock jitter). The DAC coefficients were scaled as a compromise between dynamic range, SNR, stability and power consumption. The optimized coefficients were obtained using Matlab/Simulink simulations of the new architecture.

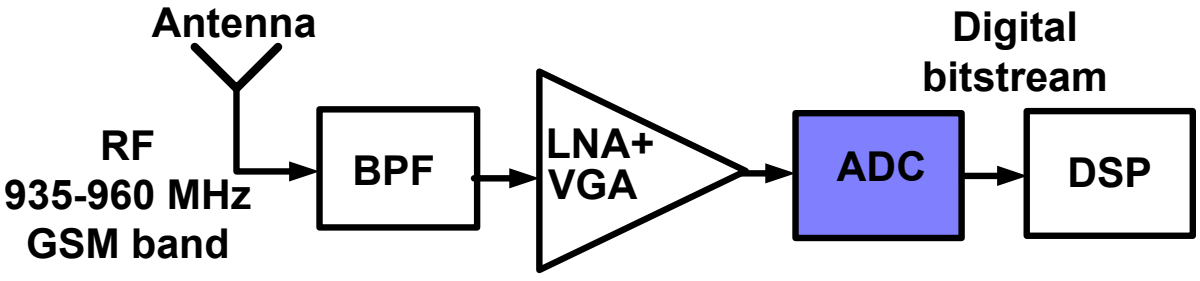

Fig 1 Software radio receiver architecture

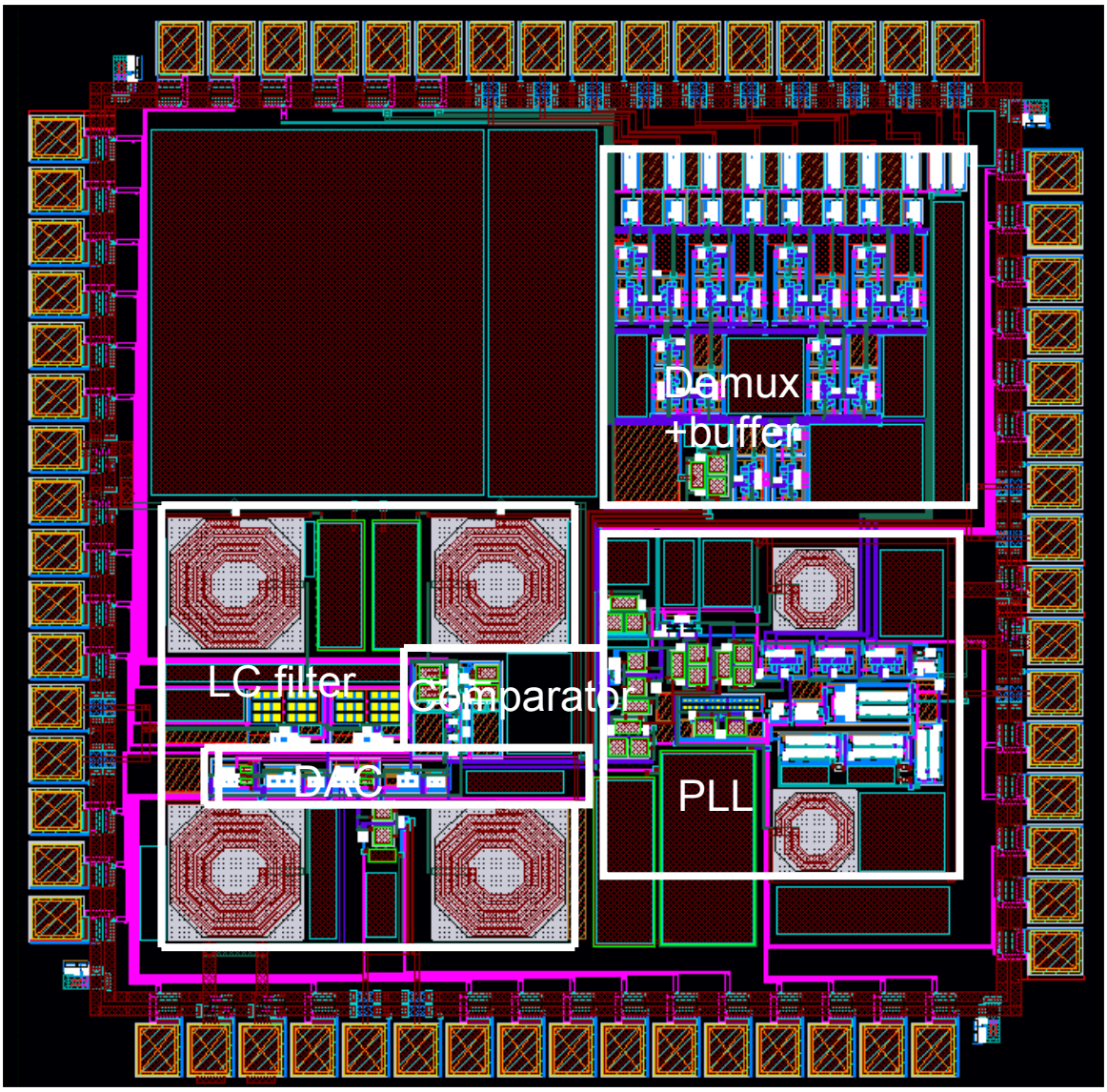

Fig 2 Layout of the system (ADC + PLL + Demux)

Status of the project

The chip is currently under characterization. Preliminary results show good SNR for the output bit stream.