High Frequency and High Dynamic Range Integrated Continuous-Time Filters.

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Abstract.
The goal of this research is to improve the dynamic range of integrated continuous time filters in order to achieve a feasible integration in next generation communication systems. This comprises the implementation and analysis of novel linearization techniques with good noise and power performance for frequencies up to 40 Mhz.

Description.
Orthogonal Frequency Division Multiplexing (OFDM) and Discrete Multi-tone (DMT) are the preferred modulation schemes currently used in DSL, PLC (Homeplug 1.0) and Wireless LAN for high data transfers. The advantages of OFDM and DMT are its flexibility, good noise immunity and it can be optimized for line conditions. The drawback, is that the large peak to average ratio of these signals demands very large dynamic range circuits (considering the fact that there is a possibility where the peaks of all carriers coincide at one point in time producing a very large signal).

This high dynamic range requirement presents a challenge in the design of integrated continuous time filters because of the unfeasible implementation of inductances (L) for frequencies below 1Ghz due to large area requirements and low Q factors. For this reason, inductances are emulated with active components (transistors) in conjunction with capacitances. The non-linearity and noise generated by these components limit the dynamic range.

Lower input referred noise levels can be achieved with higher power consumption but there is a boundary in terms of power availability and thermal dissipation. It is then desirable to apply larger input signals for improved signal to noise ratios. However, as the input signal is larger, the non-linear behavior of active components introduces intermodulation components acting as noisy interferers. The above dilemma pushes for the search of efficient linearity enhancement circuit techniques.

In this research, improved transconductors have been proposed for the implementation of linear OTA-C filters. These include proposed techniques such as non linearity cancellation using double differential pair, triple differential pair, non-linearity injection and non-linear source degeneration.

Figure 1 shows the chip microphotograph of a 30 Mhz 5^{th} order elliptic filter in a 0.35 μm CMOS technology. The topology is based on a ladder implementation using OTA based gyrators to emulate inductors. Thanks to a special linearization technique, linearity is improved by more than 10dB with almost no penalty in power consumption and noise. A self-bias circuit optimizes the linearity of the OTA and reduces its sensitivity against process tolerances and temperature variations. Filter's terminations are realized by using poly resistors instead of OTA emulation resulting in savings in power, noise and better linearity. Capacitor arrays are provided for frequency tuning; the banks are controlled with a digital code.

Figure 2 shows a comparison plot with recent publications. A figure of merit based on the spurious-free dynamic range (SFDR) per miliwatt of power per filter's order is used. It can be noticed that the performance of the proposed solution is significantly better than the trend-line.

Status of the project.
Chip fully characterized, paper is under preparation.

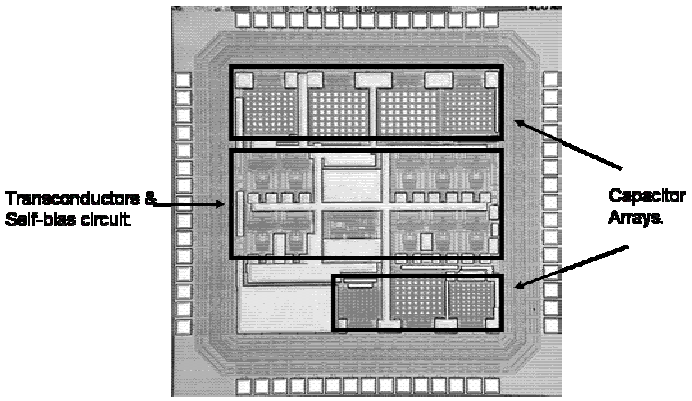

Figure 1. Layout of the filter.

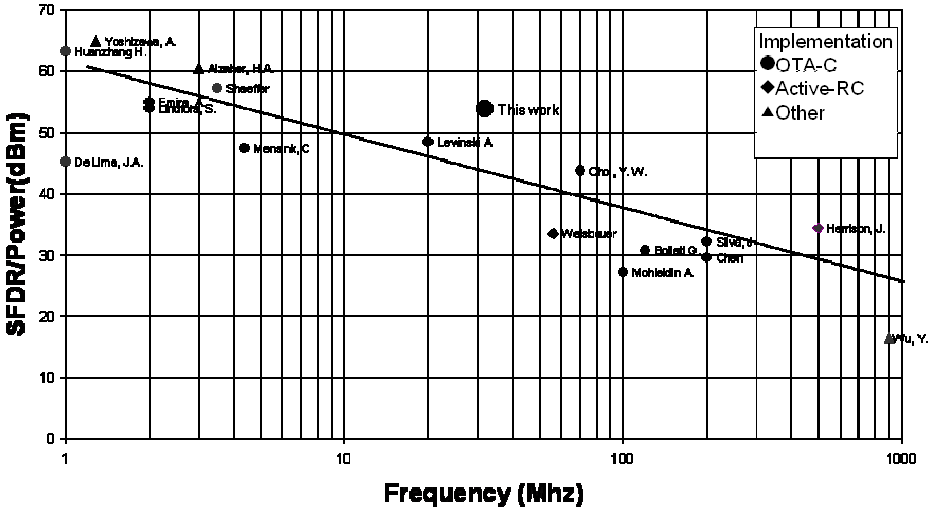

Figure 2. Performance comparison with recent publications.