DEVELOPMENT AND IMPLEMENTATION OF BUILT-IN TESTING TECHNIQUES FOR ANALOG AND RF INTEGRATED CIRCUITS

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Abstract

The objective of this research is to develop built-in testing (BIT) techniques for the functional verification of analog and RF circuits and systems. The aim is to avoid the use of external analog instrumentation so that the cost of testing is reduced. The major challenges addressed by this work are: (1) To develop techniques for the on-chip test of integrated RF and analog circuits through a fully digital off-chip interface. (2) To develop methodologies for the use of the proposed techniques in the efficient testing of integrated systems. (3) To realize and evaluate integrated implementations of the BIT architectures in a mainstream CMOS technology. At the circuit-level design, the emphasis is placed on attaining compact and robust BIT building blocks which can operate without significantly affecting the performance of the circuit under test (CUT).

Description

Three different techniques for the on-chip characterization of analog and RF circuits have been developed and experimentally demonstrated with integrated prototypes in standard CMOS technologies:

- A fully integrated **spectrum analyzer based on switched capacitor techniques** was developed, implemented and tested [1, 4]. The proposed technique for built-in testing enables the magnitude and harmonic distortion characterizations of an analog device under test (DUT) through a fully digital interface. A prototype in CMOS 0.5um technology employs 0.5mm^2 of area. With respect to the existent implementations for analog built-in testing designed in similar technologies, the proposed architecture is a more cost-effective solution (due to its robustness and, low area and low processing overhead) for characterizations in the range of MHz that do not require a dynamic range higher than 50dB [4].

- A robust technique for **on-chip magnitude and phase response characterization** based on an analog multiplier was proposed [1, 2]. Its usefulness was demonstrated experimentally in the testing of a commercial analog IC [2]. Based on this approach, a fully integrated transfer-function characterization system with a digital interface was developed, implemented and tested [6, 7]. A complete prototype in CMOS 0.35um technology employs 0.3mm^2 of area; it includes signal generator with digital control, a successive approximation ADC and the amplitude and phase detector. The operation of this built-in testing architecture is demonstrated by performing the transfer-function characterizations at various nodes of 2 different DUT (integrated in the same chip) in a range of 1 to 130MHz.

- One of the important contributions of this work is the set of building blocks developed for the implementation of the above-mentioned architectures. These circuits include three different on-chip signal generators [3, 4, 6], an analog multiplier for accurate phase measurements [2] and a compact 7-bit successive approximation ADC [6].

- Until now, mostly indirect methods have been reported for the characterization of RF circuits and systems. The on-chip characterization of RF signals has been avoided because of two main reasons (1) The inherent challenge involved in the design of circuits at high frequencies and (2) The sensitivity of the RF DUT to the additional parasitic load and noise that may be introduced by the testing circuitry. In order to address these problems a compact **CMOS RF RMS Detector** has been developed [5]. It generates a DC voltage proportional to the RMS voltage amplitude of an RF signal. A methodology for the use of this device in the built-in measurement of the gain and 1dB compression point of an RF circuit has been proposed [5]. The very small input capacitance (<15fF) and small silicon area (0.03mmsq.) of this RF RMS detector make it suitable for the direct observation of multiple high-frequency nodes and fault detection in RF systems such as a wireless transceiver. The effectiveness of the proposed device and its associated RF built-in testing technique is demonstrated by performing the characterization of a 2.4GHz LNA integrated on the same chip [7].

Status: Characterization of final IC prototypes in progress.

Publications

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[4] M. G. Mendez Rivera, A. Valdes-Garcia, J. Silva-Martinez and E. Sanchez-Sinencio, "An On-Chip Spectrum Analyzer for Analog Built-In Testing", *Journal of Electronic Testing: Theory and Applications*, Vol. 21, No. 3, pp. 205-219, June 2005.

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[6] A. Valdes-Garcia, J. Silva-Martinez, E. Sanchez-Sinencio, R. Venkatasubramanian, R. Srinivasan and F. Hussein, "Implementation of Built-In Testing Techniques for Analog and RF Circuits", submitted for *SRC TECHCON Conference, 2005*.

[7] A. Valdes-Garcia, J. Silva-Martinez, E. Sanchez-Sinencio and Faisal Hussein, "An Fully Integrated Transfer Function Characterization System", In preparation for *IEEE Journal of Solid-State Circuits*.