

Low-Power, Programmable, Low Dropout Regulator for Portable Applications

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Abstract.

This work demonstrates a technique to design a Low Power Low Dropout Regulator that eliminates the dependence on the ESR of the load capacitor. The LDO proposed in this research utilizes a fast-transient feedback loop in order to improve transient response and guarantee stability. Specifically, the main parameters to be improved are stability over the entire current range, reduced overshoot and undershoot variations, reduction of LDO deflection voltage and minimization of standby current. The LDO will also be programmable to a variety of output voltage levels while maintaining stability. The chip will be fabricated in a typical TSMC 0.35um process.

Description:

Power management is under increasingly tighter performance specifications as the market for portable electronics continues to grow at a rapid pace. The circuits in these portable electronics must operate with minimal power and maximum performance, hence, the need for low power solutions in a wide spectrum of applications. The demand in increase in battery life points to an increase in efficiency of the circuits using that battery as their power supply.

Low noise power supplies have become an integral part of today's portable applications because of the noise sensitive RF circuits that are used in hand-held electronics. The LDO (Low Dropout Regulator) has become the most popular type of linear regulator in use today due to its increase in efficiency which in turn implicates a cost of jeopardizing its stability.

The increase in efficiency translates to a larger pass element to reduce V_{dssat} . The increase in size causes a larger variation in output impedance. The large variation of load current corresponds to a drastic change in the dominant pole location, from a few hertz to the tens of kilohertz range.

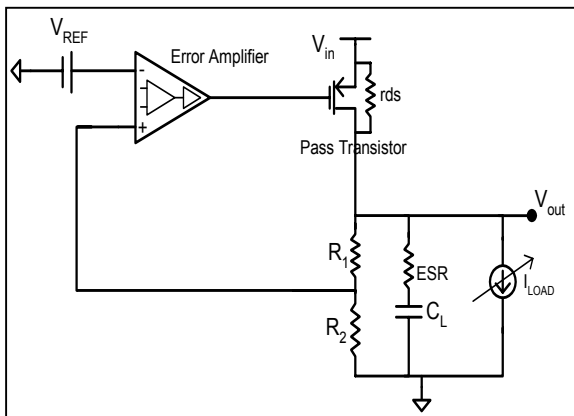


Figure 1 Typical LD

Figure 1 shows a typical LDO with an ESR modeled along with the load capacitor. This ESR will indeed stabilize the LDO, but will not improve transient response. The ESR ranges specified by the manufacturer usually require a Tantalum capacitor which in turn increases the financial cost of the overall system. Figure 2 shows the result of a transient simulation with and without an ESR for the typical LDO. The simulated voltage settings are the following: $V_{in} = 1.8V$ and $V_{out} = 1.5$.

As can be seen in figure 2 there are voltage spikes of around ~ 23 mV. These spikes can be minimized, and the dependence on ESR can be replaced by a fast transient loop that will not increase power consumption.

A compensation scheme has been developed under the premise of low power and improvement for the spikes noticeable in figure 2. It is clear that stability and transient response improvements are required in order to deem the compensation valuable.

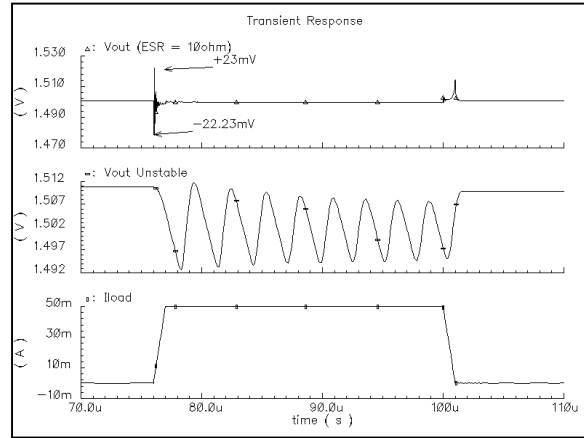


Figure 2 Transient Response

Figure 3 shows the system level schematic of the Compensated LDO. The ESR is replaced by an on-chip loop regarded as fast because its path doesn't include the relatively slow error amplifier.

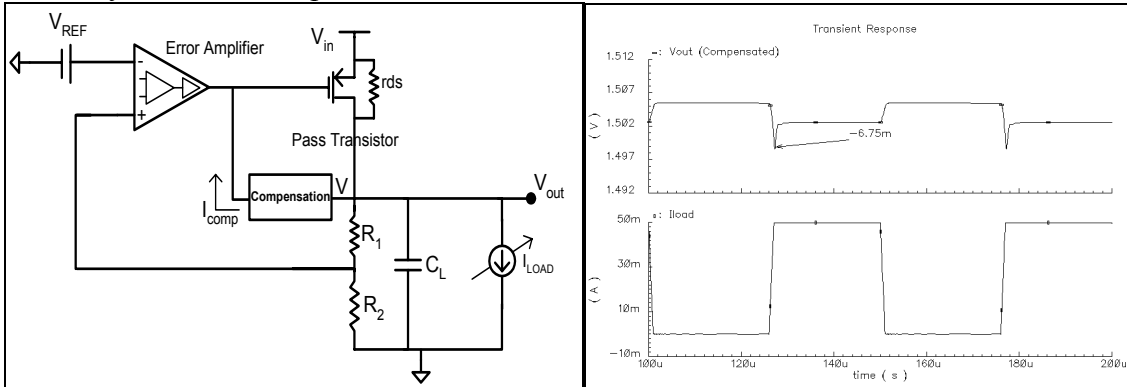


Figure 3 Compensated LDO

Figure 4 Transient Response

After simulations an improvement in transient response is clearly noticeable. These changes in transient response occur because this loop acts faster (i.e. fewer poles in path) than the loop comprised of the resistors and error amplifier. This is accomplished without a detrimental expenditure of power $\sim 38\mu A$ in total. Figure 4 shows the transient simulation results. It can be seen from these simulations (at transistor level) that the LDO functions with improvements in transient response that can correlate back to improvements in stability and phase.

Status:

It is expected that the finalized LDO be programmable for different output voltages assuming a minimum ~ 200 mV dropout voltage. It should be stable for all cases and dissipate no more than $50\mu A$ of quiescent current. The layout of two LDO's with different compensation topologies is currently underway.