

Fall 2007  
MTF 11:30-12:20  
ZEC 128-A

# ELEN 620 Network Theory: IC Design for Broadband Communication Circuits

**“An aggie does not lie, cheat, steal, or tolerate those who do”**

Instructor: Jose Silva-Martinez  
Office: 318-D, Wisenbaker Engineering Research Center (WERC)  
Phone: 845-7477  
Office Hours: 15:00-18:00 Monday and Wednesday  
Email: [jsilva@ee.tamu.edu](mailto:jsilva@ee.tamu.edu)  
**Website:** [amesp02.tamu.edu/~jsilva/](http://amesp02.tamu.edu/~jsilva/)

Textbook: **Class notes and technical papers (JSSC and TCAS-II)  
Design of Integrated Circuits for Optical Communications; B. Razavi, McGraw Hill  
book company, 2003.**

## References:

- [1] F. M. Gardner, “Phase Lock Techniques,” Wiley, New York, 3rd edition, 2003.
- [2] R. E. Best, “Phase Locked Loops: Theory, Design and Applications,” McGraw Hill, New York, 1984.
- [3] Analysis and Design of Analog Integrated Circuits, Paul Gray and Robert Meyer and Paul Hurst, John Wiley and Sons, fourth edition.
- [4] Technical papers

Objectives: To discuss circuit techniques for broadband analog integrated circuits for communication applications. The PLL architectures will be studied, and design trade-offs will be further discussed Basic amplifiers, transimpedance amplifiers, limiting amplifiers, VGAs, phase and frequency detectors, loop filters, voltage controlled oscillators and phase locked loops will be studied. Frequency synthesizers, Clock and data recovery systems will be treated as well. Most of the simulations will be done on CADENCE, Matlab, System view, and other dedicated software packages.

## Grading

Exams	60 %	
Homeworks	20 %	
Final Project	20 %	Power Point presentation.

**Grading:**

**3 midterms; no final. Closed book exams with only 1 cheating page (both sides).**

**No late homeworks!**

A → Grade  $\geq 85$

B →  $85 > \text{Grade} \geq 75$

C →  $75 > \text{Grade} \geq 65$

D →  $65 > \text{Grade} \geq 50$

F →  $50 > \text{Grade}$

# Outline

## I Introduction

## II Broadband amplifiers (lecture notes)

- Common-gate configuration
  - Impedance matching
  - Voltage gain
  - Noise figure
  - Linear range and  $P_{-1dB}$
- Common-emitter configuration
  - Impedance matching
  - Voltage gain
  - Noise figure
  - Linear range and  $P_{-1dB}$
- Differential circuits
  - Impedance matching
  - Voltage gain
  - Noise figure
  - Linear range and  $P_{-1dB}$

## III Variable gain amplifiers and Translinear Circuits (lecture notes + IEEE papers)

- Variable gain amplifier
  - Voltage gain
  - Noise figure
  - SNR
- Translinear circuits
  - Voltage gain
  - Linear range
  - Comparison with source degeneration and trade-offs
  - Noise figure
- Gilbert Cell and Mixers
  - Single ended structure
  - Impedance matching
  - Noise figure
  - Design trade-offs

## VI Data Communication Systems (Razavi)

- Channel limitations and capacity
- Random signals
  - Intersymbol interference
  - Bandwidth limitations and its effects on ISI
  - Phase noise
  - Jitter
- ISI and jitter
- Transimpedance Amplifiers
- Limiting Amplifiers

## V Phase locked loop: system's fundamentals (Gardner)

- Properties of PLLs
- Basic PLL configuration
  - Open and Closed loop transfer function
  - Stability
  - Impulse and pulse response
  - Locking and capture range
- Charge pump based PLL
  - Architectures
  - Basic building blocks
  - Capture and locking range
- Design examples and simulations

#### VI PLL building Blocks (Gardner and IEEE papers)

- Analog and Digital PLLs
- Phase and frequency detectors: Linear and digital
- Loop Filter
- VCOs
- Current-Mode Logic
- De(Serializer)
- LDVS Drivers

#### VII Applications

- Linear CDR (Razavi)
- Bang-Bang PLLs (Papers)
- Equalizers (IEEE papers)

## Tentative schedule

Section	Date
I. Introduction	
II. Broadband amplifiers	
III. Variable gain amplifiers and Translinear Circuits	
<b>1<sup>st</sup> Midterm</b>	<b>Monday 09/24</b>
IV Data Communication Systems (Razavi)	
V. Phase locked loop fundamentals	
<b>2<sup>nd</sup> Midterm</b>	<b>Friday 10/26</b>
VI. PLL building Blocks (Gardner and IEEE papers)	
VII. Applications: CDRs	
<b>3<sup>rd</sup> Midterm</b>	<b>Wednesday 11/29</b>
<b>Project presentation</b>	<b>To be decided</b>