

# ELEN 474: Analog VLSI

**“An aggie does not lie, cheat, steal, or tolerate those who do”**

Fall 2007  
MWF 10:20-11:10  
ZEC 223-B

Instructor: Jose Silva-Martinez  
Office: 318-D, Wisenbaker Engineering Research Center (WERC)  
Phone: 845-7477  
Office Hours: Monday and Wednesday: 14:00-18:00  
Email: [jsilva@ece.tamu.edu](mailto:jsilva@ece.tamu.edu)  
**Website:** [amesp02.tamu.edu/~jsilva/](http://amesp02.tamu.edu/~jsilva/)

Textbook: **Lecture notes available on Website**

Recommended Books: **Analog Integrated Circuit Design, D. A. Johns and K. W. Martin, John Wiley & Sons, 1997.**  
Design of Analog CMOS Integrated Circuits, B. Razavi, McGraw-Hill, New York 2001.  
Analysis and Design of Analog Integrated Circuits, Paul Gray, Robert Meyer and Paul Hurst and S. Lewis, John Wiley and Sons, fourth edition, 2003.

Additional References:

- [1] CMOS Circuit Design, Layout, and Simulation, R. J. Baker, H. W. Li, D. E. Boyce, IEEE Press, 1998.
- [2] Low-Voltage Low-Power Integrated Circuits, E. Sanchez-Sinencio and A. Andreou, Editors, IEEE Press, 1999.
- [3] Selected Journal Papers.

Objectives: **To discuss basic transistor models and layout techniques for the design of analog integrated circuits, and to characterize them.**

**To study the most important building blocks in CMOS technologies and understand their limitations.**

**To design analog IC circuits considering practical design parameters.**

**To use the IC design tools, especially Cadence, Spectre, Spice, and Matlab. WE expect to fabricate and test some basic CMOS ICs.**

## Grading

Laboratory	25 %	
Exams	50 %	
Homeworks	15 %	
Final Project	10 %	Power Point presentation.

Grading: Two different scales will be used for undergraduate and graduate students.  
Graduate (undergraduate) grades:

- A → Grade  $\geq 90$  (85)
- B →  $90$  (85) > Grade  $\geq 80$  (75)
- C →  $80$  (75) > Grade  $\geq 70$  (65)
- D →  $70$  (65) > Grade  $\geq 55$  (50)
- E →  $55$  (50) > Grade

**Closed book exams with only 1 cheating page (both sides)**

No late homeworks!  
No late lab reports!  
No final exam (**3 midterms**)

## Outline

### I Introduction and MOS models

- Basis of CMOS Technology
- Basic equations for the MOS transistor
- Model level 3
- Second order effects
- SPICE parameters
- Design examples

### II CMOS technologies and Layouts

- CMOS technology
- CMOS Layout and Design Rules
- Layout considerations (transistors, capacitors, resistors and inductors)
- Latch-up considerations

### III Current Mirrors and differential pair

- Basic amplifier
- Ideal and Basic current mirror
- Basic amplifiers using current mirrors (design considerations, and evaluation techniques)
- High-output impedance current mirrors
- High dc gain amplifiers (cascode, folded-cascode, triple cascode, and regulated cascode)
- Current mirror characterization techniques (DC and AC)
- Differential pair
- Frequency response
- Noise considerations
- Class AB amplifiers
- Design examples

### IV Voltage references and Differential pairs (\* most of this material is taken from Gray's book)

- Supply independent current sources (\*)
- Bootstrap Biasing (\*)
- Temperature coefficient (\*)
- Bandgap references (\*)
- Differential Pair (large signal characteristics)
- Differential Pair (small signal characteristics)
- Frequency response (dc gain, poles and zeros)
- Node impedances, low-frequency and high-frequency poles
- Design examples

### V OTA Design

- First stage
- DC considerations
- AC considerations
- Noise considerations (noise sources)
- Output and input referred noise
- Global design strategy
- Three Current Mirror OTA

- Cascode output stages
- Folded-cascode OTA
- OTA characterization

#### VI Design of a Miller OPAMP

- First stage
- Output stage
- DC considerations
- Stability considerations
- Settling time and slew-rate
- DC offset and PSRR
- Noise considerations
- Design strategy

#### VII Advanced techniques

- Enhanced output stages
- Fully-differential structures
- Common-mode feedback: limitations and design techniques
- Phase compensation techniques
- Linear OTAs: Continuous-time circuits
- Linearization techniques: IM3 and Source degeneration
- Tuning techniques
- Design examples

## Tentative schedule

Topic	Relevant Dates
I Introduction and MOS models	
II CMOS Technologies & Layouts	
<b>Review Session</b>	<b>Friday 09/21</b>
<b>1<sup>st</sup> Midterm</b>	<b>Monday 09/24</b>
III Current Sources & Diff pair	
IV Voltage references, bandgaps and differential pairs	
V Design of OTAs (first part)	
<b>Review Session</b>	<b>Wednesday 10/24</b>
<b>2<sup>nd</sup> Midterm</b>	<b>Friday 10/26</b>
V Design of OTAs (second part)	
VI Design of a Miller OPAMP	
VII Advanced techniques	
<b>Review Session</b>	<b>Monday 11/27</b>
<b>3<sup>rd</sup> Midterm</b>	<b>Wednesday 12/29</b>
<b>Project presentation</b>	<b>To be decided</b>