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ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

Room 119A ZEC

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Fault-Tolerant ASIC

Design, Implementation, and Verification

by
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Abstract: The sensitivity of application specific integrated circuits (ASICs) to the single event effects (SEE) can induce failures of the systems which are exposed to increased radiation levels in the space and on the ground. A design methodology for a full fault-tolerant ASIC that is immune to the single event upsets (SEU) in sequential logic, the single event transients (SET) in combinatorial logic and the single event latchup (SEL) in CMOS logic will be presented. The dual modular redundancy (DMR) and a SEL power-switch (SPS) are the basis of a modified ASIC design flow that incorporates the fault tolerance. Measurement results that prove the correct functionality of DMR and SPS circuits, as well as a high fault tolerance of implemented ASICs along with moderate overhead in respect of power consumption and occupied silicon area will be analyzed.

The fault injection models for simulation and validation of the fault tolerance of redundant systems to the SEUs and SETs will be introduced. The fault models are based on the random generated SEUs in sequential logic and SETs in combinatorial logic. The analytical models for calculation of the probability of failure-free triple modular redundant (TMR) and dual modular redundant (DMR) circuits will be defined. To justify the reduced redundancy concept, the simulated and calculated probabilities of failure-free TMR and DMR circuits will be discussed and compared. The results showing trade-off between hardware overhead and circuit failure-free probability of the two concepts will be presented too.

The irradiation test results of SPS circuits, obtained at the Radiation Effects Facility at the Cyclotron Institute of the Texas A&M University in College Station, will be discussed in the conclusion.

Dr. Zoran Stamenković is with IHP GmbH, Frankfurt (Oder), Germany. He received his Ph.D. degree in electronic engineering from the University of Niš, Serbia in 1995. Dr. Stamenković has published the six book chapters and more than 100 scientific journal papers, conference papers, and invited talks in the field of design and test of integrated circuits and systems.

His research interests include hardware/software co-design, SOC design for wireless communications, fault-tolerant circuits and systems, and integrated circuit yield and reliability modelling. He serves as a program committee member of many scientific conferences (among them DDECS, MWSCAS, and IPFA) and a member of the editorial board of Journal of Circuits, Systems, and Computers. Dr. Stamenković is the general chair of the 18th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems. He is a senior member of the IEEE.