

## SEMINAR

Room 1020 ETB

March 8, 2019, 1:50 – 2:50 P.M.

### MASH CONTINUOUS-TIME DELTA-SIGMA MODULATORS<sup>1</sup>

by

Jose Silva-Martinez  
Texas A&M University  
Department of ECE

**Abstract:** The emerging 5G wireless standards and broadband WiFi short range high-data rate communications demand of ultrahigh performance broadband analog-to-digital converters (ADCs). The continuous-time delta-sigma modulator (CT- $\Delta\Sigma$ ) is the popular architecture of choice for its high dynamic range (DR) capability, robustness, implicit anti-aliasing behavior, and tolerance of out-of-band blockers. To boost user throughput and increase network capacity, lower power (P), wider bandwidth (BW) low-pass CT- $\Delta\Sigma$ s are critical building blocks in the modern direct conversion receivers

The multi-stage noise-shaping (MASH) topology cascading low-order single-loop modulators has recently gained popularity. Compared with high-order single-loop implementations, MASH CT- $\Delta\Sigma$ s show superior stability and overload recovery capability. Therefore, MASH modulators tolerate more out-of-band noise and show a potential of wide-bandwidth and low power capability. Nevertheless, the noise leakage due to poor matching between analog and digital transfer function and the non-ideal inter-stage interfacing exists as the main limitations of the MASH CT- $\Delta\Sigma$  topology.

To exploit the MASH CT- $\Delta\Sigma$  architecture to its full potential, the aforementioned issues are analyzed and addressed employing innovative design techniques at both system and circuit levels. This seminar focuses on the design of MASH CT- $\Delta\Sigma$  architectures. Three silicon proof design examples (if time permits) demonstrating the suitability of the proposed techniques are presented.

---

The emerging 5G wireless standards and broadband WiFi short range high-data rate communications demand of ultrahigh performance broadband analog-to-digital converters (ADCs). The continuous-time delta-sigma modulator (CT- $\Delta\Sigma$ ) is the popular architecture of choice for its high dynamic range (DR) capability, robustness, implicit anti-aliasing behavior, and tolerance of out-of-band blockers. To boost user throughput and increase network capacity, lower power (P), wider bandwidth (BW) low-pass CT- $\Delta\Sigma$ s are critical building blocks in the modern direct conversion receivers

The multi-stage noise-shaping (MASH) topology cascading low-order single-loop modulators has recently gained popularity. Compared with high-order single-loop implementations, MASH CT- $\Delta\Sigma$ s show superior stability and overload recovery capability. Therefore, MASH modulators tolerate more out-of-band noise and show a potential of wide-bandwidth and low power capability. Nevertheless, the noise leakage due to poor matching between analog and digital transfer function and the non-ideal inter-stage interfacing exists as the main limitations of the MASH CT- $\Delta\Sigma$  topology.

To exploit the MASH CT- $\Delta\Sigma$  architecture to its full potential, the aforementioned issues are analyzed and addressed employing innovative design techniques at both system and circuit levels. This seminar focuses on the design of MASH CT- $\Delta\Sigma$  architectures. Three silicon proof design examples (if time permits) demonstrating the suitability of the proposed techniques are presented.

---

<sup>1</sup> Qiyuan Liu, Alexander Edward, Carlos Briseno-Vidrios and Jose Silva-Martinez, "Design Techniques for MASH Continuous-Time Delta-Sigma Modulators," Springer, New York, NY. Book, 250 pages, 2018.  
In memory to Alex