Analog and Mixed-Signal Center
3128 TAMU
College Station, TX 77843-3128
Tel. (979) 862-4253
Fax. (979) 845-7161
E-mail: hoyos@tamu.edu

ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

Room 1020 ETB

March 22, 2019, 1:50 – 2:50 P.M.

Design of Power Efficient Pipeline Analog-to-digital Converters and a Digitally-assisted Dual-loop LDO

by

Dadian Zhou
Texas A&M University

Abstract: In recent years, the demand of portable electronic devices grows rapidly, including mobile phones, laptops, smart devices, etc. All of these devices have batteries providing limited power. Therefore, power-efficient designs for integrated circuits on those devices become a popular topic, e.g. highly power-efficient ADCs. Moreover, portable devices, such as mobile phones, switch commonly between different modes. This requires fast regulators to provide enough current for those modes. Thus, a fast linear regulator with low quiescent current is highly demanded as well. To follow the trend, two projects will be discussed in the seminar.

One of our projects is about a pipeline ADC with current-mode multiplying digital-to-analog converters (MDACs). The current-mode MDAC architecture is proposed and is compared with a conventional flip-around switch-capacitor MDAC. The residual amplifier in current-mode architecture will save large amount of power theoretically. The work eventually achieves 68-dB/82-dB SNDR/SFDR at 260MS/s with a sinusoidal input. The total power consumption is 15.4mW. The area of ADC core is 0.276 mm^2 and is fabricated in TSMC 40nm technology. The other research is a design of a digitally-assisted dual-loop LDO. A digital loop in the LDO is turned on when a large current load step occurs. The digital loop is realized by using a 3-bit flash ADC directly controlling 7 segmented pass transistors. When the digital loop enters a steady state, the flash ADC output will jump between 1 LSB. In this case, the loop controller activates an analog loop and disables the digital loop. In the analog loop, an error amplifier is used for loop settling. Therefore, the proposed dual-loop LDO has no output ripples compared with conventional digital LDOs.

Dadian Zhou (S'17) received his B.S. degree in Telecommunication Engineering from Xi'an Jiaotong-Liverpool University, Suzhou, Jiangsu, China and earned his M.S. degree in Communications and Signal Processing from Imperial College London, London, UK. Since 2014, he has been pursuing his Ph.D degree in Electrical Engineering in Analog and Mixed Signal Center, Texas A&M University, College Station, TX, USA. He worked as an Analog Engineering Intern with NXP Semiconductors, Austin, TX, in Summer 2017 and Summer 2018, where he was involved in general purpose IO design and verification. He was a recipient of Broadcom scholarship in 2014. His research interests include data converters, calibrations for analog and mixed-signal systems, power management (LDO design) and IO design.