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ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

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PWM Technique with Time-Ratio Duty Cycle Computation

by

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Abstract: Many applications require conversion of an analog signal to an accurate PWM output. Low cost integrated circuits need a very cost-optimized solution that does not compromise on the accuracy of the PWM output.

Our solution to this problem consists off a simple, minimal analog circuitry controlled by a small digital core. The core also processes the pulses generated by in the analog block.

A first rising edge of one input to the core, as result of a ramp signal crossing a first reference voltage starts the PWM conversion. It is followed by a second rising edge corresponding to the ramp crossing the analog signal to be converted. Finally, the last tripping of the signal at the input of the core, as result of the same ramp crossing a second reference voltage, concludes the PWM conversion.

The digital core, after computing the duty cycle using a high frequency clock, outputs a new PWM signal with the desired output frequency and the computed duty cycle.

Paul Vulpoiu received a MS degree from Polytechnic Institute of Bucharest, Romania and his PhD from UPIT, Romania.

With experience in designing from electronic equipment for nuclear applications to CMOS imagers, controllers for optical devices, power management ICs and drivers, he co-authored nine patents and three technical books.

Currently he is a Senior Analog Designer in Motor Drive Department of Texas Instruments in Dallas.

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