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ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

Room 1035 ETB

April 9, 2018, 1:50 – 2:50 P.M.

High PSR and Fast Settling Time Techniques in Low Dropout Voltage Regulators

by

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Abstract: Nowadays power management systems are an important part of integrated systems. To power sensitive analog systems, efficient low-noise voltage regulators are required. These regulators are usually a combination of efficient switching converters and low dropout (LDO) voltage regulators. A brief discussion on the basics of LDOs, techniques to improve power supply rejection (PSR), settling time, and overall regulation are going to be discussed in this presentation.

Fernando Lavalle-Aviles received his B.Sc. degree in electrical engineering from the Instituto Tecnologico de Merida (ITM), Yucatan, Mexico. In Fall 2011, he joined the Analog and Mixed Signal Group (AMSC) at Texas A&M University, College Station, USA, where he is currently pursuing his Ph.D. in electrical engineering. From Fall 2011 until Summer 2016, he was a scholarship holder from the Consejo Nacional de Ciencia y Tecnologia (CONACYT) of Mexico. From Fall 2016 to date he holds the TI Excellence Fellowship. His research interests include LDOs, active-RC filters and class-D audio amplifiers.