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**ELECTRICAL & COMPUTER
ENGINEERING**
TEXAS A & M UNIVERSITY

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On-Chip Two-Tone Synthesizer Based on a Mixing-FIR Architecture

by

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Abstract: A low-distortion current-steering two-tone sinusoidal signal synthesizer based on a mixing-FIR architecture is proposed. The proposed robust synthesizer adopts only digital blocks. It implements a two-stage cascade FIR harmonic cancellation technique that generates a single tone quasi-sinusoidal waveform and suppress the odd-order harmonics up to the 21st order. Differential-mode circuitry and a 50% duty cycle clock are also utilized to cancel the even-order harmonics. The single-tone signal is further up-converted to the desired LO frequency band, thereby producing the desired two-tone sinusoidal signals. The proposed synthesizer contains a current mirror array implementing the FIR tap coefficients. Accuracy is enhanced using dynamic element matching. The other building blocks consist of a 24-phase clock generator, a current combiner, and a passive mixer with bootstrapped MOS switches. This twotone synthesizer can be used to conduct a linearity built-in self-test. It is fabricated in 130 nm standard CMOS technology, occupying a 0.056 mm² silicon area. Measurement shows better than -68 dBc IM3 below 480 MHz LO frequency without calibration. For the LO frequency < 76.8 MHz and the two-tone difference < 2 MHz, an IM3 better than -75 dBc can be achieved. The imbalance between the two-tone amplitudes is measured < 0.1 dB across the whole frequency range.

Congyin Shi was born in Fuzhou, Fujian, China. In 2008 and 2011, He received his bachelor degree and the M.Sc. degree of Microelectronics from Peking University, Beijing, China. He is currently pursuing the Ph.D. degree in the Analog and Mixed-Signal Center at Texas A&M University, College Station, USA. He worked at Google Inc. for summer internship in 2015 and 2016. His current interests are in the area of mixed-signal built-in self-test, analog circuit on-chip optimization, integrated signal generator and frequency synthesizer.