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ELECTRICAL & COMPUTER ENGINEERING
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Enabling Design Virtualization for VLSI Circuits

by

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Abstract: Advanced geometry nodes present numerous choices for the VLSI circuit designer. These include process variants, transistor channel lengths, VT types, library tracks, memory compilers and operating voltage to name a few. Optimization across all these variables is not practical due to the complexity of VLSI design. At eSilicon, we have developed an innovative methodology called design virtualization that allows the designer to predict the behavior of a complex VLSI design across these variables in minutes. In Virtualization, we implement the design virtually using different combinations of these variables and enumerate them in the order of the optimization criteria. Virtualization is based on a large design database that consists of thousands of simulations of test circuits ranging from small structures to large building blocks. The virtualization process examines key design metrics associated with a design to find the best correlation of a target design with the designs in the design database. Using this approach, we have successfully optimized power and performance for several production designs in 40nm and 28nm at eSilicon.

Prasad Subramaniam received a Ph.D. in Electrical Engineering at Stony Brook University NY in 1982. He spent 16 years at Bell Laboratories in Murray Hill NJ where he was responsible for analog, RF and TCAD design tools. From 1998 – 2000, he was at Cadence Design Systems as a Vice President of R&D responsible for analog and mixed signal simulation. Since 2000, he has been with eSilicon where he is responsible for Design Technology and R&D.