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ELECTRICAL & COMPUTER ENGINEERING
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S E M I N A R

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Wearout and Lifetime in Future Chip-Multiprocessor Interconnect

by

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Abstract: Moore's Law scaling is continuing to yield even higher transistor density with each succeeding process generation, leading to today's multi-core Chip Multi-Processors (CMPs) with tens or even hundreds of interconnected cores or tiles. Unfortunately, deep sub-micron CMOS process technology is marred by increasing susceptibility to wearout. Prolonged operational stress gives rise to accelerated wearout and failure, due to several physical failure mechanisms, including Electromigration (EM), Hot Carrier Injection (HCI) and Negative Bias Temperature Instability (NBTI). Each failure mechanism correlates with different ambient and usage-based stresses, all of which can eventually generate permanent faults. While the wearout of an individual core in many-core CMPs may not necessarily be catastrophic for the system, a single fault in the inter-processor Network-on-Chip (NoC) fabric could render the entire chip useless, as it could lead to protocol-level deadlocks, or even partition away vital components such as the memory controller or other critical I/O. In this talk, I examine wear mitigation along two axes: first, we address NBTI wear in the microarchitectural structures of the on-chip router. We show NBTI wear is correlated with lack of use of components of the router's critical path. We then develop a technique to maximally increase utilization of that critical path as a way to reduce wear. Second, we address EM and HCI wear at the full network level. We show that EM and HCI wear on the links is highly related to the temperature of the cores. We then develop a wear-mitigating, globally adaptive routing function that routes packets away from temperature hotspots on the chip to reduce the impact of EM and HCI wear.

Paul V. Gratz is an Associate Professor in the department of Electrical and Computer Engineering at Texas A&M University. His research interests include energy efficient and reliable design in the context of high performance computer architecture, processor memory systems and on-chip interconnection networks. He received his B.S. and M.S. degrees in Electrical Engineering from The University of Florida in 1994 and 1997 respectively. From 1997 to 2002 he was a design engineer with Intel Corporation. He received his Ph.D. degree in Electrical and Computer Engineering from the University of Texas at Austin in 2008. His papers "A Control-Theoretic Approach for Energy Efficient CPU-GPU Subsystem in Mobile Platforms" and "B-Fetch: Branch Prediction Directed Prefetching for Chip-Multiprocessors" were nominated for best papers at DAC '15 and MICRO '14 respectively. At ASPLOS '09, Dr. Gratz received a best paper award for "An Evaluation of the TRIPS Computer System." In Spring 2010, he received the "Teaching Excellence Award - Top 5%" award from the Texas A&M University System for a graduate-level computer architecture course he developed.