Analog and Mixed-Signal Center
3128 TAMU
College Station, TX 77843-3128
Tel. (979) 845-9586
Fax. (979) 845-7161
E-mail:kentesar@ece.tamu.edu

ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY

S E M I N A R

Room 1003 ETB

April 16, 2015 3:55-5:10 P.M.

High-Speed and Low-Power Wireline and Wireless Communication IC Design

by

Ping Gui
Southern Methodist University

Abstract: The rise of cloud computing and mobile communications has driven an explosion in the need for data communication bandwidth, making efficient wireline and wireless transceivers capable of operating at the limits of the process technology increasingly critical.

On the wireline front, new communication standards have pushed the data-rates to 25-28 Gb/s. For such high-speed data-links, it is highly desirable not only to obtain high performance, but also to keep the power consumption low for integration of multiple channels on a single chip and integration with the digital processing circuitry. Low-voltage (LV) operation of the front-end receiver circuitry is very attractive from the perspective of both low-power operation and integration with the digital circuitry. While the use of low supply voltage is a common approach to lower the power consumption for digital circuitry, it is difficult for a LV front-end receiver to achieve low phase noise (PN), low jitter, low Bit-Error-Rate (BER) and wide data-rate range. In the first half of the talk I will present our very-low-voltage low-power clock-data-recovery (CDR) circuit, where we explore circuit techniques that enable the entire CDR to operate at half of the nominal supply voltage to achieve both high-speed and low power operation. Implemented in a 65 nm CMOS process, the 25 Gb/s CDR together with an equalizer consume a total power consumption of 55.4 mW under a 0.6 V supply voltage, achieving a power efficiency of < 2 mW/Gb/s.

On the wireless communication front, millimeter-wave (mmWave) 60GHz and above) technologies using CMOS have been an active research area in both academia and industry for their capability of accommodating wide bandwidths, high antenna gain, and small form factor. In the second half of the talk, I will present our recent research results on mmWave IC design including V-band and W-band VCO, Quadrature VCO (WVCO), LNA and Power Amplifiers. New circuit design techniques to improve the phase noise, noise figure, power gain, and power efficiency of the above key building blocks will be presented along with silicon measurement results.

In the end of the talk I will briefly talk about my other on-going and future research projects related to mixed-signal high-speed and mmWave IC design.

Dr. Ping Gui is an Associate Professor of Electrical Engineering in the Lyle School of Engineering at Southern Methodist University, Dallas, TX. She received her Ph.D. degree in Electrical and Computer Engineering from the University of Delaware, and joined the Faculty of Lyle School of Engineering at SMU in 2004. Her research interests include analog, mixed-signal, and RF/mmWave IC design for a variety of applications including high-speed wireless and wireline communications, medical devices, automotive RADAR, and circuits and systems for harsh environments. Dr. Gui is a senior member of IEEE, a recipient of CERN Scientific Associate Award (2008-2011), IEEE Dallas Section Outstanding Service Award (2011), and the SMU Ford Research Fellowship Award (2015).